Electrical characterization of gate dielectrics for 4H-SiC MOSFETs

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Faculty of Physical Sciences
University of Iceland
2017

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Dissertation submitted in partial fulfillment of a
Philosophiae Doctor degree in Physics

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Reykjavik, December 2017

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Bibliographic information:
Rabia Yasmin Khosa, 2017, Electrical characterization of gate dielectrics for 4H-SiC MOSFETs, PhD dissertation, Faculty of Physical Sciences, University of Iceland.

ISBN: 978-9935-9320-3-7

Printing: Háskólaprent ehf., Fálkagata 2, 107 Reykavík
Reykjavik, Iceland, December 2017

Abstract

Silicon is a semiconductor material used in most power devices and the Si metal-oxide-semiconductor field effect transistor (MOSFET) is the key switching device for high power applications. Recently silicon carbide (SiC) MOSFETs have emerged on the market for high voltage (>900 V) applications and these devices are more energy efficient than their Si counterparts. However, 4H-SiC MOSFET devices with native oxide, SiO_2, as a gate dielectric are hampered by unacceptably low electron inversion channel mobilities which severely limit the output current. This low mobility is attributed to a high density of interface traps at the SiO_2/SiC interface resulting in electron trapping and coulomb scattering at the interface. The growth or annealing of the SiO_2 layer in NO or N_2O ambient improves the interface quality but more reduction in interface trap density is still needed. Other large bandgap high k-dielectrics such as Al_2O_3, AlN, HfO_2 and ZrO_2 have been investigated in an attempt to replace SiO_2 in SiC MOS (metal-oxide-semiconductor) devices. In our work, we are dealing with Al_2O_3 and AlN as gate dielectrics and compare their electrical properties with thermally grown SiO_2. MOS capacitors with Al_2O_3 or AlN as a single layer or in stack with other different dielectrics are analyzed using capacitance-voltage (CV) and conductance-voltage (GV) techniques. We applied and developed a GV technique in order to quantify the density of so-called near-interface traps (NITs) that are located few nm within the dielectric. Our findings show that Al_2O_3 and AlN make a very good interface with SiC and the interface traps observed at the SiO_2/SiC interface are practically absent at AlN/SiC and Al_2O_3/SiC interfaces. However, current-voltage analysis shows that Al_2O_3 and AlN have relative low breakdown field (4-5 MV/cm) when grown on SiC. This problem can be greatly reduced by using Al_2O_3 or AlN in stack with large bandgap dielectric like SiO_2 which then increases the breakdown voltage of the dielectric. The findings suggest that a stack of SiO_2 with a thin layer of Al_2O_3 or AlN at the SiC interface can be a realistic alternative to sole SiO_2 as a gate dielectric in 4H-SiC MOS devices.

Útdráttur

Aflrafeindatæknin í dag byggir að miklu leyti á rafsviðssmárum (MOSFET) sem gerðir eru í hálfleiðaranum kísli (Si). Sú tækni hefur verið bestuð undanfarna áratugi og nú er svo komið að það eru efniseiginleikar kísilsins sem takmarka straumgetu og spennuþol þessara íhluta. Á síðustu árum hafa hins vegar komið fram á sjónarsviðið nýjir smárar sem gerðir eru í hálfleiðaranum kísilkarbíði (SiC) sem hafa betri nýtni en hefðbundnir kísilsmárar og leiða til umtalsverðs orkusparnaðar. Fram að þessu er þó einungis unnt að nota SiC smárana við mjög háar spennur (> 900 V). Megnið af þeim rásum sem notaðar eru í aflrafeindatækni vinna hins vegar með spennur á bilinu 400-600 V og þar eru SiC smárarnir ekki samkeppnishæfir. Ástæðan er ekki tengd efniseiginleikum kísilkarbíðsins heldur því hvernig samskeyti SiC myndar við einangrandi efnið kísildíoxíð (SiO_2) sem nauðsynlegt er til stýra smáranum. Straumgeta smárans takmarkast af því að veilur á SiO_2/SiC samskeytunum hremma rafeindir sem eru á leið í gegnum smárann sem veldur því að straumurinn er um þrefalt lægri en búast má við ef samskeytin væru gallalaus. Reynt hefur verið að leysa þetta vandamál síðustu 20 árin en ekki tekist enn sem komið er. Í þessu rannsóknarverkefni er markmiðið að leysa þetta með því að rækta aðra einangrara: álnítríð (AlN) eða áloxíð (Al_2O_3) ofan á SiC í stað SiO_2. Niðurstöður þessa verkefnis gefa tilefni til bjartsýni þar sem fjöldi veilna á AlN/SiC og Al_2O_3/SiC samskeytunum er mun minni en á hefðbundnum SiO_2/SiC samskeytum. Einnig tókst að auka spennuþol þessara samskeyta með því að bæta við einangrandi lögum ofan á Al_2O_3 og AlN lögin. Hins vegar er þörf á að leita leiða til að auka spennuþol samskeytanna enn frekar ef þessir einangrarar eiga að geta tekið við hlutverki kísildíoxíðs í aflsmárum.

Dedicated to my father Mushtaq Ahmed Khosa (late)

List of publications

Publications included in this thesis

A. **Low density of near-interface traps at the Al_2O_3/4H-SiC interface with Al_2O_3 made by low temperature oxidation of Al**
R. Y. Khosa, E. Ö. Sveinbjörnsson, M. Winters, J. Hassan, R. Karhu, E. Janzén and N. Rorsman
Materials Science Forum, ***897*** *135-138 (2017).*

B. **Conductance signal from near-interface traps in n-type 4H-SiC MOS capacitors under strong accumulation**
R. Y. Khosa and E. Ö. Sveinbjörnsson
Materials Science Forum, ***897*** *147-150 (2017).*

C. **Electrical properties of 4H-SiC MOS Capacitors with AlN gate dielectric grown by MOCVD**
R. Y. Khosa, J. T. Chen, R. Karhu, J. Hassan, N. Rorsman and E. Ö. Sveinbjörnsson
manuscript submitted for publication.

D. **Electrical characterization of amorphous Al_2O_3 dielectric films on n-type 4H-SiC**
R. Y. Khosa, E. B. Thorsteinsson, M. Winters, N. Rorsman, J. Hassan, R. Karhu and E. Ö. Sveinbjörnsson
manuscript submitted for publication.

E. **Study of near-interface traps in n-type 4H-SiC MOS capacitors from conductance signal under strong accumulation**
R. Y. Khosa and E. Ö. Sveinbjörnsson
Manuscript in preparation.

Acknowledgements

All praises and thanks are for almighty ALLAH Who is the most Gracious and Merciful. He is the most compassionate and beneficent, Who consecrated mankind with the knowledge and ability to think into his secrets. He bestows me the sense of knowledge and enables me to accomplish this task.

All respects to Holy Prophet Muhammad (peace be upon him), who directed the humanity and mankind from the world of darkness to an era of peace and enlightened the hearts with Almighty Allah’s message.

I would like to express my deep and sincere gratitude to my supervisor, Prof. Einar Örn Sveinbjörnsson, whose wide knowledge, encouragement, guidance and support from the initial to the final level enabled me to develop a better understanding of my research work.

I would like to express my best wishes to Professor Erik Janzén (late), Linköping University, Sweden, may he find peace in heaven. I am very thankful to Jawad ul Hassan, Jr Tai Chen, Michael Winters and Niklas Rorsman for help in processing my MOS samples in the clean rooms of Chalmers University and Linköping University, Sweden. Special thanks to Jawad ul Hassan for his useful advises and moral support.

I am grateful to Professor Bengt G. Svensson, University of Oslo, Norway, for providing me TDRC facility. I also much appreciate the help of Marit Larsen, Ilia Kolevatov and Hussein Ayedh during my stay in Oslo. I would like to thank Kristján Jónsson for his help in fixing a lot of lab stuffs especially TDRC setup, Einar Baldur for his help in LabView and XRD, Unnar Arnalds for his help in AFM and in thin film growth by e-beam evaporator, Tryggvi and Taha for their help in XRD, Vanik Shahnazaryan, Gunnar Arthúr and Kevin Dini for help in programming languages of Matlab and Wolfram Mathematica. I would like to convey my thanks to Bing, Ramya and Anna-Karin for their excellent company. Ramya and Bing made my lunch time awesome through the years. I want to say special thanks to Bing for her moral support all the time. Thanks to everyone in VR-III for their nice attitude towards me.

I express my warm thank to Pakistani friends, Icelandic mosque friends and Spanish speaking friends for spending unforgotten times together.

I owe my loving thanks to my mother, Taj Begum and siblings especially to Khadija Yasmin Khosa without their cooperation and encouragement it would not have been possible for me to complete my Doctorate.

The financial support is acknowledged from the Icelandic Research Fund of University of Iceland. I also gratefully acknowledge the Swedish Foundation for Strategic Research (SSF), and the MC2 Nanofabrication Laboratory at Chalmers University of Technology, Göteborg, Sweden.

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1 Motivation

The large bandgap, high breakdown field and high thermal conductivity make silicon carbide (SiC) a promising candidate for high power and high temperature electronics. The metal-oxide-semiconductor field effect transistor (MOSFET) is one of the basic building blocks of silicon based electronic circuits and currently there are no devices made in other materials that can compete with Si devices for mainstream integrated circuits. However, in power electronics SiC MOSFETs are currently being introduced to the market and such devices are competitive for blocking voltages above 900 V. In principle, such SiC devices should outperform its Si counterparts through higher energy efficiency and less need for cooling systems. In practice, the SiC MOSFETs do not yet deliver the expected output current because of poor electrical quality of the interface between the gate oxide (SiO_2) and the SiC.

The success of silicon based MOSFETs is mainly due to the high quality of the SiO_2/Si interface. The standard method to improve the quality of the SiO_2/Si interface is a post oxidation-annealing in hydrogen ambient which passivates detrimental interface states in forms of dangling silicon bonds. SiC is the only compound semiconductor that has SiO_2 as its native oxide. Studies show that the thermal oxide grown on SiC contains in some cases trace amounts of carbon but in terms of breakdown field such oxides are comparable to SiO_2 thermally grown on Si. The most critical problem of the SiC based MOSFETs is the highly defective SiO_2/SiC interface which is not improved by hydrogen post-oxidation annealing. A standard technique to grow high quality SiO_2/SiC interface does not exist today. The density of traps at the SiO_2/SiC interface is still orders of magnitude higher than at the SiO_2/Si interface. This results in low current output of SiC MOSFETs since a large amount of the inversion channel electrons are trapped in interface traps and do not contribute to the current. Furthermore, this severe electron trapping increases the coulomb scattering and severely reduces the electron mobility. For this reason, a great number of studies have been made to investigate alternative gate dielectrics for SiC MOS devices.

The aim of this work is to find the best alternative to SiO_2 as a gate dielectric and for that purpose we combine different characterization methods to understand the dielectric/SiC interface. The alternative gate dielectrics used in our study are AlN and Al_2O_3. The dielectrics were grown by various techniques such as thermal oxidation of Al (to make Al_2O_3), atomic layer deposition (ALD) and metal organic chemical vapor deposition (MOCVD) to form AlN. AlN or Al_2O_3 are used as a sole gate dielectric or in a stack with different dielectrics like SiO_2.

2 Introduction

Silicon carbide (SiC) is a crystalline compound of silicon and carbon atoms. Since the late 19th century SiC has been an important material for sandpapers, grinding wheels and cutting tools because of its hard nature. The electrical properties of SiC were first studied in the beginning of the 20th century and the first light-emitting diode was made in SiC in 1907 [1]. For solid state electronic device applications, a high quality single crystalline SiC semiconductor is required. In 1955, Lely developed a method to grow the single crystalline SiC and later the refinement of this growth method enabled the commercialization of single crystalline SiC wafers in the beginning of the 1990s. Today, three to six inch single crystalline SiC wafers can be purchased and majority of them are produced today in the United States [2].

2.1 SiC crystal structure and physical properties

SiC crystals exist in many crystalline forms or polytypes. The most commonly used SiC polytypes for research and application purposes are 6H-SiC and 4H-SiC, here "H" stands for hexagonal. The fundamental structural unit of all SiC polytypes is a covalently bonded tetrahedron of four carbon atoms with a single Si atom at the center. In the same way, each carbon atom is surrounded by four Si atoms. This is illustrated in figure 2.1.

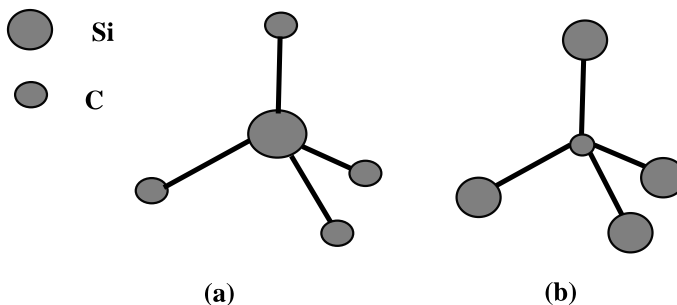


Figure 2.1 (a) A silicon atom surrounded by four carbon atoms, (b) a carbon atom surrounded by four silicon atoms.

Figure 2.2 shows that Si atoms in a plane form a hexagonal structure, for simplicity let's say plane A. Carbon atoms are positioned on the top of Si atoms in either two configurations named B and C, shown in figure 2.2 (a) and (b) respectively, also forming hexagonal matrix. A basic SiC crystal is formed by stacking hexagonal patterns of Si and C atoms on top of each other in either of the two configurations AB or AC. A variety of SiC polytypes can be generated by changing the stack order. The stacking direction is referred to as *c-axis*. The positive *c-axis* is in the direction in which Si atoms are situated in stack. In figure 2.2, the *c-axis* is pointing downwards (negative) while in figure 2.1, the *c-axis* is pointing upwards (positive). The crystal surface in figure 2.2 facing up is called the carbon

face while the surface facing down is called the silicon face. In this thesis, experiments are carried out on 4H-SiC and 6H-SiC polytypes using the Si face.

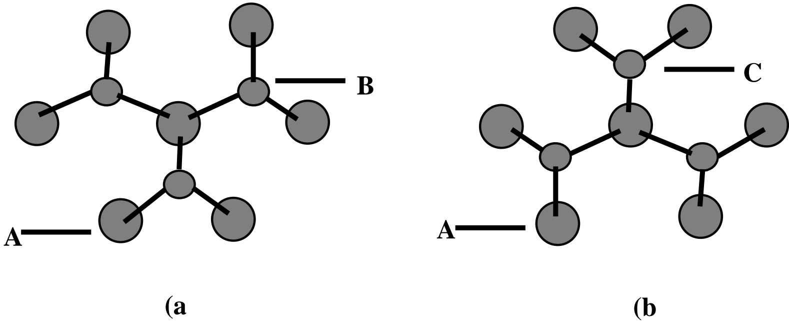


Figure 2.2 Carbon atoms are positioned on the top of a silicon hexagonal matrix in two ways. In (a) the stacking sequence is AB and in (b) the stacking sequence is AC.

In 4H-SiC and 6H-SiC polytypes, the numbers, 4 and 6, stand for the count of layers in a period. The stacking sequence in 4H-SiC and 6H-SiC is ABAC and ABCACB respectively. The stacking sequence of 4H-SiC and 6H-SiC is shown in figure 2.3 (a) and (b) respectively. Figure 2.3 (c) shows the view of hexagonal crystal from the bottom along with the vectors [1000], [0100] and [0010]. In this figure, the *c-axis* is pointing into the page. All our SiC wafers were made from ingots cut almost perpendicular to c-axis with few degrees off towards the [11$\underline{2}$0] direction. Our 4H-SiC and 6H-SiC wafers are cut 4° off-axis. This is done to conserve the polytype of the SiC during epitaxial growth.

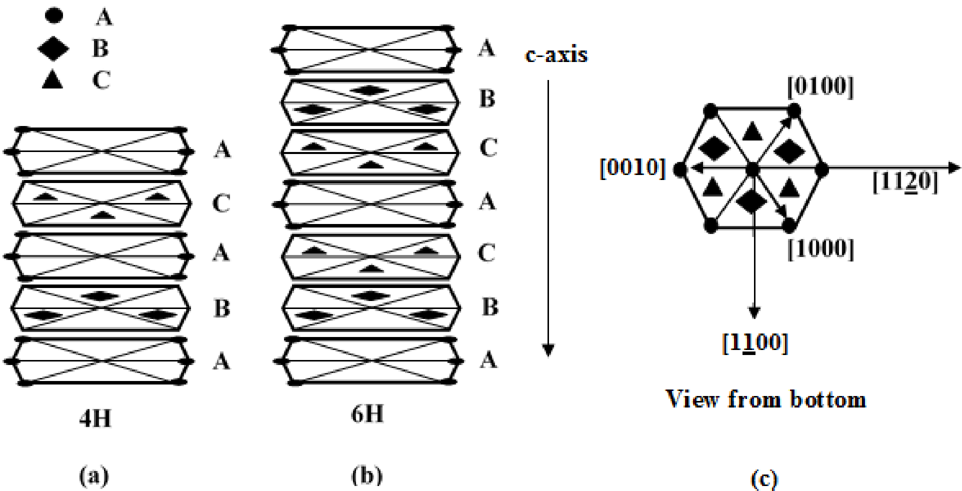


Figure 2.3 Stacking sequence of (a) 4H-SiC and (b) 6H-SiC. (c) view of hexagonal crystal from bottom with three vectors [1000], [0100] and [0010]. The directions [11$\underline{2}$0] and [1$\underline{1}$00] are also shown. The vector [0001] points into the page, in direction of negative c-axis.

Physical properties of SiC and Si are listed in Table 2.1. As it is stated in Table 2.1, the SiC is a wide bandgap semiconductor therefore SiC devices can operate at an elevated temperature while Si becomes intrinsic above 250°C. SiC has critical breakdown field which is about 10 times higher than in Si and it is this high breakdown field that enables the fabrication of high voltage and high power devices. SiC is an excellent thermal conductor (thermal conductivity around 3 times higher than Si) which allows SiC devices to have good performance at high power levels and dissipate the large amount of generated heat without any cooling system. The high saturation electron drift velocity, about 2 times higher than in Si, enables the SiC devices to operate at high frequencies.
Among the 4H-SiC and 6H-SiC semiconductors, the 4H-SiC is more isotropic and has a higher bulk electron mobility than 6H-SiC. Therefore, 4H-SiC is the more suitable candidate for device applications and the main industrial effort is currently on devices made in 4H-SiC.

Table 2.1 Room temperature physical parameters of SiC and Si with doping concentration of 10^{16} cm^{-3}. From [3].

	Si	**4H-SiC**	**6H-SiC**
Bandgap (eV)	1.1	3.26	3.0
Breakdown field (MV/cm)	0.25	2.2	2.5
Saturation velocity (10^7 cm/s)	1.0	2.0	2.0
Bulk electron mobility $\mu_e \parallel c$ (cm^2/ Vs)	1350	880	360
Bulk electron mobility $\mu_e \perp c$ (cm^2/ Vs)	-	800	97
Thermal conductivity (W/cm K)	1.5	5.0	5.0
Dielectric constant	11.9	9.7	9.7

2.2 SiC MOSFETs in power electronics

There is a high demand for transistors with high efficiency in power electronics. MOSFET is a semiconductor device which is widely used in electronics. It is a three-terminal device with source (S), gate (G), drain (D) terminals. A schematic diagram of a MOSFET is shown in figure 2.4. A MOSFET has a semiconductor layer below the dielectric layer which is located between the source and drain terminals. The semiconductor is either n-type or p-type depending on the required channel of the MOSFET. To operate MOSFETs, let’s consider an n-channel MOSFET which has p-type semiconductor underneath the gate. A positive voltage is applied to the gate terminal to invert the p-type semiconductor to n-type in the region closest to the dielectric layer. When we apply the positive gate voltage, the holes present in p-type semiconductor under the dielectric layer are pushed down with a repulsive force and a depletion region is created. The positive voltage also attracts the electrons from the n+ source and drain regions into the depletion region and a thin electron rich channel forms close to the dielectric layer. This is shown in figure 2.4 (b). Now, if a voltage is applied between the drain and source, the current flows freely between source and drain. The gate voltage controls the density of electrons in the channel. The aim of the MOSFET is to control the current flow between source and drain by the gate voltage. The MOSFET can work as switch or as a signal amplifier with the gate voltage as the input signal. The operation of the MOSFET depends largely upon the MOS capacitor. The MOS capacitor is the main part of the MOSFET that is highlighted in figure 2.4a with a broken

line. In this thesis, we are dealing with the MOS capacitors since they are the building blocks of the MOSFETs.

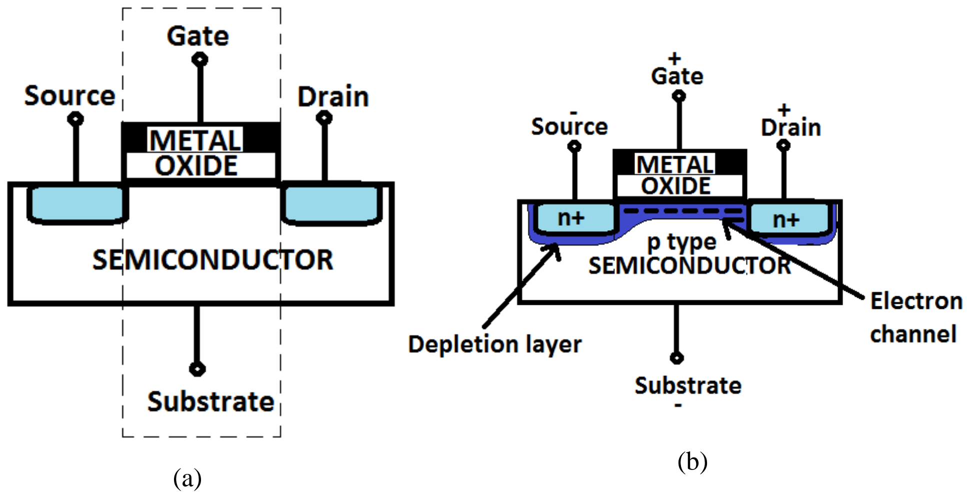


Figure 2.4 (a) A schematic diagram of MOSFET. (b) An electron channel forms in the ON-state of n-channel MOSFET.

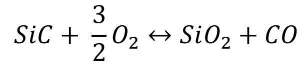
Si based MOSFET is the key switching device for most power applications. Recently, silicon carbide has gained substantial interest as a promising candidate for such applications. Energy efficient SiC MOSFETs have emerged recently on the market for high voltage (>900 V) applications [4-6]. These devices provide higher switching speed and lower switching losses compared to their Si counterparts. Currently, low voltage blocking devices made in SiC are not competitive to Si technology due to poor electron channel mobility in SiC MOSFETs which is due to electron trapping at the interface between the SiC and the native gate dielectric, silicon dioxide. Recently, a lot of work has been done on examining alternative gate dielectrics. In order to work as a proper gate dielectric, the material must have a large bandgap and act as a potential barrier for both holes and electrons. This requires conduction and valence band offsets between the dielectric and the SiC of at least 1.5 eV. The dielectrics that fulfill this criterion are Al_2O_3 (bandgap ~ 7.0 eV) and AlN (bandgap ~ 6.5 eV). Other materials like high-k materials used in search for dielectrics for Si CMOS have too small bandgaps for practical use on 4H-SiC. The interface quality of SiO_2, AlN or Al_2O_3 dielectrics with SiC is discussed in the next section.

2.3 Dielectrics

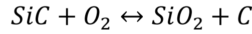
2.3.1 Silicon dioxide

The native oxide of SiC is silicon dioxide (SiO_2) which can be grown uniformly across the SiC surface by thermal oxidation. SiC is an inert material and it oxidizes very slowly at temperatures below 1000°C. The oxidation rate of SiC depends on the crystal orientation and the oxidation rate of C-face SiC is almost one order of magnitude higher than that of

the Si-face [7]. The dependence of oxidation rate on the crystal orientation is attributed to the polarity of tetrahedral bonding during the oxidation reaction [8]. During dry oxidation of SiC, the following chemical reactions occur [8]:

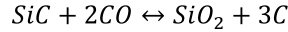


$$SiC + \frac{3}{2}O_2 \leftrightarrow SiO_2 + CO$$

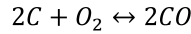


$$SiC + O_2 \leftrightarrow SiO_2 + C$$

The amount of remaining carbon in the oxide is controlled by the following reactions



$$SiC + 2CO \leftrightarrow SiO_2 + 3C$$



$$2C + O_2 \leftrightarrow 2CO$$

Generally, it is believed that most of the carbon is removed from the SiO_2 as CO gas. It has also been observed that during oxidation carbon penetrates into SiC and reduces the number density of intrinsic carbon vacancies. An important deep level defect $Z_{1/2}$ has been assigned to the carbon vacancy and this defect acts as a very effective recombination center and limits the minority carrier lifetime in 4H-SiC [9]. Presence of carbon at the SiO_2/SiC interface has also been detected in some studies even though its concentration away from the interface is reported to be below the detection limit for Auger electron spectroscopy [10] and X-ray photoelectron spectroscopy (XPS) [11,12]. It has been proposed that carbon accumulates at the SiO_2/SiC interface and forms carbon clusters which result in the creation of interface states [13]. The amount of carbon close to the SiO_2/SiC interface is very difficult to determine because of the high carbon background in the SiC.

Afanas'ev et al. proposed that a dominant portion of interface states is because of two sources i.e. interfacial carbon clusters and traps in the oxide [13]. It is suggested that the interfacial carbon clusters either form sp^2-bonded clusters or graphite-like clusters when they are in large concentrations. The energy spectrum of sp^2-bonded carbon clusters can be exemplified as a band in the lower half of the SiC energy bandgap as they grow up to graphite-like clusters, the band extends to the upper part of SiC energy bandgap [13]. The presence of sp^2-bonded carbon clusters at the SiO_2/SiC interface was first suggested on the base of internal photoemission (IPE) measurements [13]. Later, the presence of C-related particles was also observed on the SiC surface by atomic force microscope (AFM) after removing the SiO_2 layer [14]. The second proposed source of interface states are traps in the oxide but close to the SiO_2/SiC interface. Before discussing the oxide traps and their effect on device performance it is important to know that the electrically active traps close to the dielectric/SiC interface are generally classified into interface traps and near interface traps (NITs). The interface traps are located exactly at the dielectric/SiC interface while NITs are located at some distance (1-2 nm) inside the dielectric [15]. The location of such traps is illustrated in figure 2.5. Afanas'ev et al. observed the presence of NITs at the SiO_2/SiC interface by using photo stimulated electron tunneling [16]. Later Saks et al [17] supported the presence of these NITs by performing low temperature capacitance-voltage measurements on SiC MOS devices.

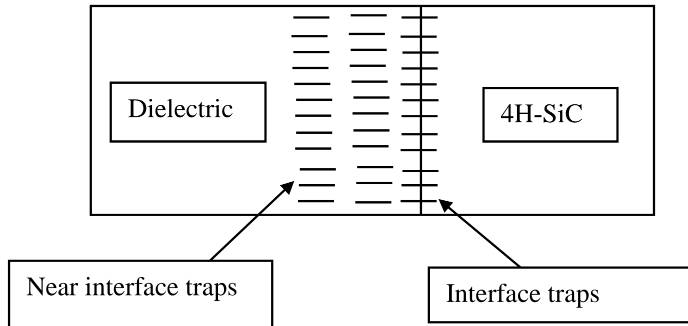


Figure 2.5 Schematic overview of the distribution of traps close to the dielectric/SiC interface.

SiO_2 has a significant density of electrons traps about 2.8 eV below its conduction band. These oxide traps are considered to be native in SiO_2 and are associated with oxygen vacancies [13,18,19]. In the case of SiO_2 grown on SiC, the defects are reported in the transition region near the SiO_2/SiC interface [20,21] and their possible origins are oxide-carbon bonds [22] or carbon vacancy oxygen complexes at the interface [23]. Such oxide traps, being close to conduction band of SiC, are believed to be the main cause of low channel mobility particularly in 4H-SiC n-channel MOSFETs (i.e. < 20 cm^2/Vs) [24-26] while in 6H-SiC, these traps are above the SiC conduction band minima and they only respond when the 6H-SiC MOS device is in strong accumulation. This reflects the fact why 6H-SiC MOSFETs in general have higher channel mobility than the ones made in 4H-SiC [25, 27-29]. Oxygen vacancy-related traps are also observed at SiO_2/Si interface [30] but they are located well above the conduction band of Si and do not restrain the performance of Si MOSFETs.

Attempts to improve the SiO_2/SiC interface

For making SiC MOSFETs, the 4H-SiC polytype is preferred to 6H-SiC because of its higher and more isotropic bulk electron mobility. However, the large density of interface traps close to the conduction band of 4H-SiC are a serious obstacle for developing MOS devices. Different methods have been used to improve the SiO_2/SiC interface:

- Possible carbon clusters are the result of incomplete oxidation of carbon at the SiO_2/SiC interface. Direct deposition of SiO_2 on SiC using e.g. remote plasma enhanced chemical vapor deposition [31] or jet vapor deposition techniques [32] has been performed and the results are not satisfactory.
- Post-oxidation annealing in the presence of pyrogenic stream (H_2+O_2) and at temperatures below the oxidation temperature of SiC reduce the density of deep interface traps. It is thought this reduction is due to reduction of the amount of carbon at the interface [27]. Kosugi et al [33] showed that by optimizing the water vapor contents the SiO_2/SiC interface quality can improve while Ólafsson et al

[34,35] observed that this post-oxidation annealing reduces the density of deep traps but it increases the density of shallow traps that limit the electron mobility.

- Post-oxidation annealing in hydrogen at a high temperature improves the interface and enhances in some cases the channel mobility of MOSFETs [36-39].
- Annealing or growth of the oxide in the presence of nitric oxide (NO) or nitrous oxide (N_2O) gas improves the interface quality by reducing the density of traps close to the conduction band of SiC [19, 40-42]
- Different ionic impurities have been used to passivate the interface traps, for example P [43,44], Rb, Cs, Ba and Sr [45-47], As and Sb [48,49], La [50], and B [51,52], K [53] or Na [54,55]. Although such impurities improve the interface quality the appearance of polarization charges (in case of phosphorus) close to the interface or the movement of impurity charges during device operation bring variation in threshold voltages of the MOSFETs that are unacceptable for practical applications.

The quality of the SiO_2/SiC interface has been improved to some degree using various techniques as mentioned above and has enabled the commercialization of the high voltage (> 900V) SiC MOSFETs. Mostly the commercial SiC devices use nitride (N_2O or NO) oxides. These high voltage devices can tolerate lower mobilities than the low voltage ones (400 V - 900 V) because the current in high voltage devices is limited by the resistance of the low doped SiC used in these devices. However, for low voltage devices a reduction in the interface state density near the conduction band is needed to achieve an acceptable electron channel mobility. The high-volume market in power electronics are devices blocking 400 V - 900 V and this market is estimated to be about four times larger than that for devices above 900 V [56].

2.3.2 Aluminium oxide

Aluminium oxide (Al_2O_3) has been investigated intensively in recent years as a potential gate oxide for SiC MOS technology. The main advantage of Al_2O_3 as a gate dielectric is the wide bandgap of ~ 7.0 eV [57-59]. The Al_2O_3 conduction band offset to 4H-SiC is ~1.6 eV [58] which is expected to be sufficient for n-channel MOSFET operation. An amorphous Al_2O_3 is a better candidate as a dielectric for SiC devices than poly-crystalline α-Al_2O_3 because of leakage through grain boundaries [58].

Al_2O_3 may be deposited onto SiC using many different techniques such as plasma deposition [60], thermal oxidation of metallic Al film [61], metal-organic chemical vapor deposition (MOCVD) [62] and atomic layer deposition (ALD) [58,63-65]. The ALD technique has received the largest interest despite the fact that as grown ALD Al_2O_3 typically contains a large amount of negative charges which are reduced only after annealing at 1000°C [63,64]. Thermal oxidation of metallic Al film has been investigated in some detail. The studies show that for temperatures below 300°C an amorphous Al_2O_3 film of uniform thickness is formed. At higher oxidation temperatures, an amorphous Al_2O_3 film initially develops and then gradually transforms into crystalline γ-Al_2O_3 [61].

Some very promising results were obtained by introducing a thin SiO_2 interfacial layer to the SiC underneath the Al_2O_3 layer [62,65]. A very high peak field effect mobility of 300 cm^2/Vs is achieved in SiC MOSFETs using Al_2O_3 made by MOCVD with a thin SiO_2 interfacial layer to the SiC [62]. However, the mobility drops very rapidly with gate

voltage and is less than 50 cm^2/Vs at moderate gate voltages and this work has not been repeated. Most recently, pre-deposition surface cleaning and post deposition annealing at different temperature in N_2O ambient has been performed on ALD grown Al_2O_3. As a result of post deposition annealing at 1000°C, a thick interfacial SiO_x ($0 < x < 2$) layer grows containing a high density of interface traps [66]. Similar observations are made when reactive ion sputtered Al_2O_3 grown at room temperature is annealed in oxygen at 1100°C [67]. Amorphous Al_2O_3 has been used recently as a gate dielectric in graphene field effect transistors with some success [68,69]. In summary, the potential of the Al_2O_3/SiC system has been examined in a number of studies but further investigations are still needed to test its usefulness in high power and high temperature electronics.

2.3.3 Aluminium nitride

The other proposed dielectric material for SiC is aluminium nitride (AlN). The bandgap of AlN of 6.2 eV [70-73] is smaller than Al_2O_3 and SiO_2. A lattice mismatch to SiC of only 1% and a high dielectric constant of about 8 are the encouraging points. This 1% lattice mismatch to SiC enables a single crystalline growth of AlN films on SiC substrates [73]. AlN has been investigated on 4H-SiC and the reported conduction and valence band offsets are 1.7 eV and 1.3 eV respectively as determined by XPS [74].

There are not many studies on electrical characterization of AlN layers on SiC. However, SiC MOSFETs with crystalline AlN as a gate dielectric grown by molecular beam epitaxy (MBE) have been reported but the structures were leaky and the channel mobility was very low (< 1 cm^2/Vs) [75,76]. Fixed charge and interface traps are important issues in AlN/SiC MOS devices [73,77]. Initial pre-irradiation of atomic nitrogen before AlN film growth and a flow of ammonia during temperature ramp-up results in an improvement of the insulating quality of the AlN film [77,78]. There is one report on the introduction of a thin SiO_2 layer between SiC and AlN as an additional barrier to prevent electron injection from the semiconductor to the dielectric and less charge injection was observed when 100 Å SiO_2 layer was used. [79].

3 Experimental methods

3.1 Samples preparation

In our study, AlN or Al_2O_3 dielectric are prepared on n-type epitaxial layers grown on highly nitrogen doped ~ $1x10^{18}$ cm^{-3} n-type 4H-SiC wafers via several methods. The epitaxial layers are 10 µm thick with a net doping concentration of nitrogen of ~ $1x10^{16}$ cm^{-3} grown on 4 degrees off-axis 4H-SiC substrates. Prior to dielectric deposition all samples are cleaned with HF in order to remove the native oxide. The preparation of AlN or Al_2O_3 as a sole or in stack with different dielectrics is summarized as follows. After deposition of the dielectric layers circular MOS pads are made using Al as a gate metal. The backside contact is formed by thick Ni (100nm) or Al (500 nm) metallization.

3.1.1 Growth methods of Al_2O_3 and its stack layers

Al_2O_3 growth

Hot plate method: 1-2 nm thick Al metal layer was deposited by electron beam evaporation of Al in a vacuum chamber at a rate of 0.5 A/s and then immediately the sample is baked on a hot plate at a temperature of 200°C-300°C for 5 minutes to form the Al_2O_3 layer. This cycle is repeated several times to achieve a final thickness of Al_2O_3 between 6 and 15 nm.

Atomic layer deposition (ALD): Al_2O_3 was deposited at 300°C via thermal decomposition of $Al_2(CH_3)_6$ in water ambient.

Rapid thermal processing (RTP): Four samples of Al_2O_3 were prepared by oxidation of pure Al metal and subsequent rapid thermal annealing in oxygen ambient at 500°C, 600°C, 700°C, and 1000°C for 30 min, 30 min, 15 min, and 5 min respectively.

Stack growth

SiO_2/Al_2O_3 stack: SiO_2 was grown by plasma enhanced chemical vapor deposition (PECVD) at 300°C using source gases of oxygen and silane. Al_2O_3 was grown by the hot plate method.

3.1.2 Growth methods of AlN and its stack layers

AlN growth

Metal organic chemical vapor deposition (MOCVD): AlN was grown in a horizontal hot-wall metal organic chemical vapor deposition (MOCVD) reactor at 1100°C. Ammonia and $Al_2(CH_3)_6$ were used as precursors for N and Al.

Stack growth

SiO_2/AlN stack: SiO_2 layer was deposited by PECVD at 300°C using source gases of oxygen and silane. AlN was grown by MOCVD at 1100°C.

Al_2O_3/AlN stack: Al_2O_3 was deposited by ALD at 300°C and AlN was grown by MOCVD at 1100°C.

Si_3N_4/AlN stack: Si_3N_4 layer was made by low pressure chemical vapor deposition (LPCVD) at 770°C using source gases of ammonia and silane. AlN was grown by MOCVD at 1100°C.

SiO_2/Si_3N_4/AlN stack: Si_3N_4 layer was made by LPCVD at 770°C and SiO_2 layer was deposited by PECVD at 300°C. AlN was grown by MOCVD at 1100°C.

3.2 Characterization techniques

AlN/SiC or Al_2O_3/SiC interfaces have been investigated by performing electrical measurements on MOS capacitors. The electrical characterization techniques used are discussed below.

3.2.1 Capacitance- voltage measurements

Capacitance-voltage (CV) measurement is the most used method to determine the interface quality of MOS capacitors. It is a time saving and a rather easy method to obtain the interface state density close to the conduction band of n-type SiC at the dielectric/SiC interface. We utilize two different CV measurement methods. Firstly, we measured the capacitance versus voltage at different frequencies, ranging from 1 kHz to 1 MHz, and at different temperatures ranging from 100 K to 400 K. Here we obtain an estimate of the energy distribution of interface traps. Secondly, we measure the CV relationship when the sample is cooled from room temperature down to 77 K while maintaining a certain charging voltage on the gate. Then sequentially the gate bias is swept from negative bias to forward bias. This method is used to determine the effective trapped charge at the dielectric/SiC interface and this provides a certain estimate of the density of NITs.

CV measurements at different frequencies

The first estimate of the number density of interface states in MOS capacitors can be made by investigating the frequency dispersion of the CV curves. Electron capture into interface states is most often a fast process (takes typically less than a microsecond) while electron emission from interface traps is normally much slower and is a thermal process which depends on the energy difference E_c-E (where E is the energy level of the interface trap and E_c denotes the SiC conduction band edge). If an electron is captured and not emitted again this is detected as a shift of the CV curve to higher gate voltage. If the test frequency is high (1 MHz) then more traps will not emit their electrons and the curve is shifted to the right as compared to the low frequency (1 kHz) curve [15]. This frequency shift can clearly be seen in figure 3.1, which indicates that this MOS sample with thermally grown SiO_2 grown in O_2 has a significant amount of interface traps.

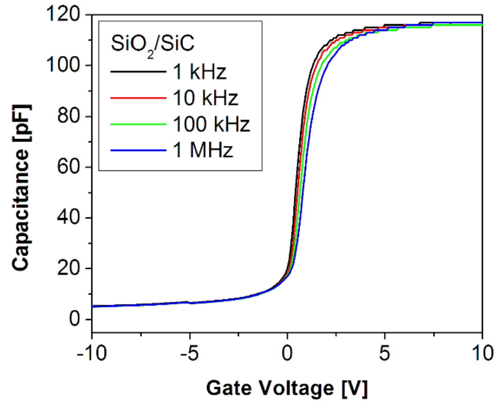


Figure 3.1 Room temperature CV spectra of a MOS sample with thermal SiO_2 grown in O_2. (at 1150°C for 90 min) at four test signal frequencies from 1 kHz to 1 MHz.

From the frequency dispersion of CV spectra as shown in figure 3.1, it is possible to estimate the interface trap density (D_{it}) using the expression [15]

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1-C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1-C_{hf}/C_{ox}}\right) \qquad (3.1)$$

where, C_{ox} is the oxide capacitance, q is the elementary charge, C_{lf} is the capacitance at low frequency and C_{hf} is the capacitance at high frequency. In our case, we are using the frequency range 1 kHz to 1 MHz. It is very common to use a much lower frequency of 1 Hz or lower in so called quasi-static CV measurements where D_{it} values then tend to be a bit higher because more traps can follow the quasi-static signal as compared to 1 kHz [15]. It should be pointed out that our method is not accurate for obtaining absolute values of the interface state density but can be used to compare interface state densities in differently prepared dielectrics. An example of D_{it} as a function of energy from the SiC conduction band edge is given in figure 3.2. The energy scale from the SiC conduction band edge is estimated by assuming a constant capture cross section of traps of ~ 10^{-17} cm^2 for all energy levels. This figure shows that the SiO_2/SiC interface has high density of interface traps close to SiC conduction band edge.

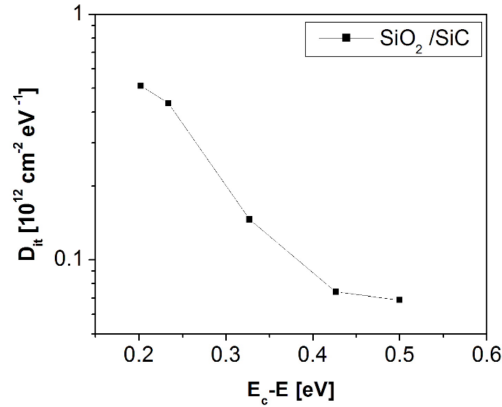


Figure 3.2 Density of interface states (D_{it}) as a function of energy from the SiC conduction band edge, extracted from CV data in figure 3.1.

Low temperature CV measurements with increasing electric field across the dielectric

The interface traps capture electrons very rapidly and their density can be determined by conventional CV at room temperature as mentioned above. However, the density of NITs is usually underestimated in such analysis since the density of trapped electrons in NITs depends strongly on the field across the dielectric and the room temperature CV technique is not sensitive at high accumulation bias [80]. An estimate of the charge trapped in NITs can be obtained from CV analysis when the sample is cooled from room temperature down to 77 K while maintaining a certain charging voltage on the gate. The NITs are filled under strong accumulation and the number density of trapped electrons increases with increasing accumulation bias. If the sample is cooled to 77 K under accumulation bias, most of the captured electrons remain trapped in the NITs and then give a positive shift in the flatband voltage during subsequent CV measurement at 77 K [80]. The example of such analysis is shown in figure 3.3 (a) for SiO_2/SiC MOS sample. The number density of accumulation (N_{acc}) electrons and of trapped electrons (N_{it}) at the interface is then determined by using the expression

$$N_{it} = \frac{C_{ox}\left(V_{FB(G)} - V_{FB(T)}\right)}{qA} \quad , \quad \mathrm{N_{acc}} = \frac{\mathrm{C_{ox}}\left(\mathrm{V_{(G)}} - \mathrm{V_{FB(T)}}\right)}{\mathrm{qA}} \tag{3.2}$$

where $V_{FB(G)}$ and $V_{FB(T)}$ are the flat band voltages at different charging voltages and at charging temperature respectively, q is the absolute value of electron charge and A is the gate area. $V_{(G)}$ denotes the applied gate voltage during cooling. This method is used to determine the number density of accumulated and trapped electrons at the interface as a function of the electric field across the oxide during charging. The result of such analysis is shown in figure 3.3 (b)

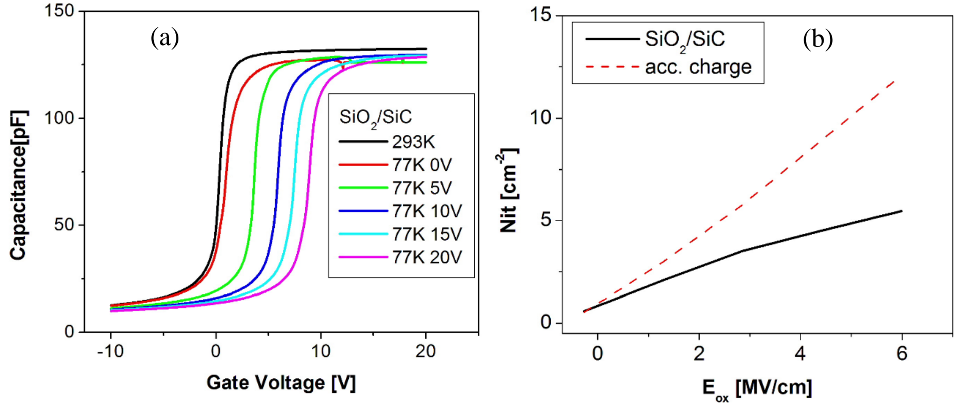


Figure 3.3 (a) CV curves (100 kHz) of SiO_2/SiC MOS capacitor taken at 77 K using different charging bias (0-20 V) during cooling down to 77 K. (b) Number density of trapped charge (N_{it}) in interface states (black curve) as a function of the field across the oxide (E_{ox}) during charging, extracted from CV data in (a). Dotted line shows the number density of the accumulation charge for a given gate voltage during cooling.

3.2.2 Investigation of electron trapping deep inside the dielectrics

In the literature, it is common to observe large flatband voltage shifts in the CV curves upon repeated measurements for n-type 4H-SiC MOS devices that have AlN or Al_2O_3 as a dielectric [73,77,63,64]. Such a shift, as compared to the theoretical curve, is even observed for fresh capacitors and has then been attributed to the presence of fixed negative charges within the dielectric but has not been investigated carefully [63,64]. In our MOS samples of AlN and Al_2O_3, such CV shifts were not observed on fresh pads but only after repeated CV sweeps and the shift then saturates after several sweeps. An example of this is shown in figure 3.4. Our findings, in papers C and D, show that the shift in the CV curve is not because of fixed negative charges but rather because of trapping of free electrons from the SiC within the dielectrics. These trapped electrons can easily be emitted back to the SiC by using two techniques (a) depletion bias stress and UV light illumination and (b) depletion bias stress while raising the temperature. Both these techniques are discussed below.

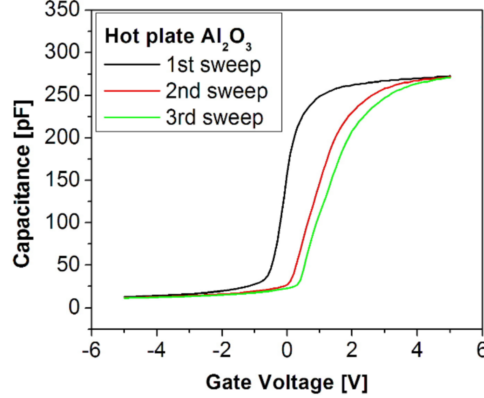


Figure 3.4 CV spectra of an Al_2O_3 sample upon repeated CV sweeps from depletion to accumulation. The shift of the CV curves is due to trapping of electrons within the Al_2O_3 under strong accumulation bias which saturates after several sweeps.

CV measurements applying depletion bias stress and UV light illumination

The existence of electron capture and emission from traps within the gate oxide can be examined by applying depletion bias stress and ultraviolet (UV) light illumination. In this measurement, first the traps within the gate oxide are intentionally filled by applying accumulation bias stress to the MOS capacitors for a certain period. Under this action, the electrons are injected into the oxide and the trapped electrons are detected as a flatband shift in the following CV measurement. In a second step, the sample is illumined by UV light under depletion bias stress for certain period, afterwards a shift in flatband is again observed in the successive CV measurement but this time in the opposite direction. This indicates that electrons trapped in the gate dielectric are released during the UV exposure. The amount of the released trapped charge can be determined by using the expression

$$N_{it} = \frac{C_{ox}(V_{FB} - V_{FB(UV)})}{qA} \tag{3.3}$$

Where V_{FB} and $V_{FB(UV)}$ are flat band voltages before or after applying UV light respectively. An example of such a measurement is shown in figure 3.5. In this figure, the MOS capacitor is first kept in accumulation (+5 V) for 30 min to intentionally fill the traps in the Al_2O_3 dielectric and then the bias is swept from depletion (-5 V) to accumulation (+5 V) and the CV (black curve) is recorded. Next, a depletion bias of -5 V is applied, together with ultraviolet (UV) light illumination, for 30 min to examine if electrons are released from Al_2O_3 traps under such conditions. A flatband shift to negative gate voltage is observed in the subsequent CV sweep (red curve). This flatband shift indicates that electrons trapped in the Al_2O_3 are released during the UV exposure. From this shift in the CV curves before or after applying UV light, we can determine the amount of released electrons from the Al_2O_3 using equation 3.3.

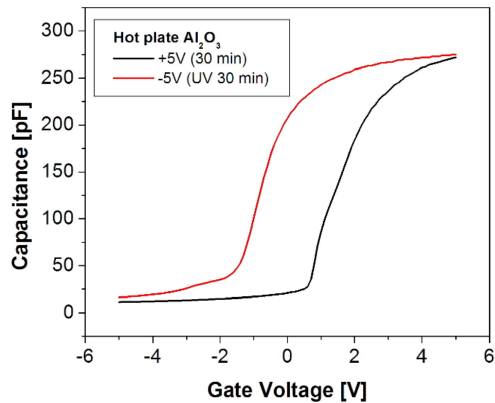


Figure 3.5 CV characteristics (100 kHz) of a hot plate Al_2O_3 sample at room temperature before and after applying bias stress or UV illumination to it. The black curve is recorded after accumulation bias stress (+5 V) while the red curve is recorded after subsequent depletion bias stress (-5 V) combined with UV light exposure of the sample.

CV measurements using depletion bias stress and raising the temperature

In this method, the electron traps within the dielectric are first intentionally filled with electrons by applying accumulation bias at room temperature to the MOS sample for a certain time. The filling of the traps with electrons is detected as a flatband shift in the following CV measurement. In the second step, the sample is kept under depletion bias stress for a certain period and at a certain temperature. Afterwards, a shift of the flatband voltage in an opposite direction is observed in the successive CV measurement. This CV analysis can be performed at different time intervals to obtain a rough estimate of the rate of emission of electrons as well using different temperatures. An example of such a measurement cycle is shown in figure 3.6. In this figure, the MOS capacitor is first kept in accumulation (+20 V) for 10 min to intentionally fill the traps in the AlN dielectric and then the bias is swept from depletion (-5 V) to accumulation (+20V) and the CV (black curve) is recorded. Afterward, the sample is kept at 360 K for 22 hours with depletion bias of 0 V. A flatband shift to low gate voltage is observed in the following CV sweep (red curve) taken after time interval of about 22 hours. This flatband shift indicates that electrons trapped in the AlN are released by raising the temperature of the sample while keeping the sample under depletion bias.

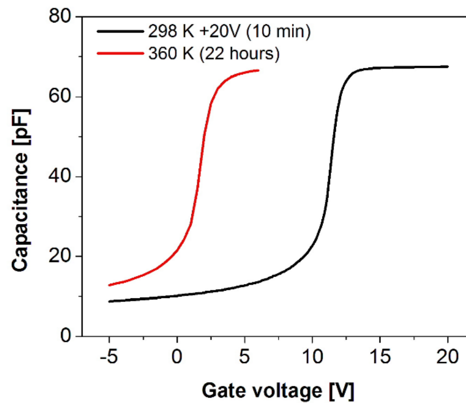


Figure 3.6 CV characteristics (100 kHz) of AlN MOS capacitor. The black curve is recorded after accumulation bias stress at room temperature while the red curve is recorded after time interval of 22 hours at a temperature of 360 K under 0 V bias.

3.2.3 Conductance-Voltage measurements

The conductance-voltage (GV) method is considered to be a more accurate method than other methods to determine the density of interface traps [15]. The analysis of experimental GV data is, however, quite tedious and time consuming. Especially, surface potential fluctuations complicate the experimental data analysis. GV measurements are made using different gate voltages and test frequencies. GV spectra of a thermally grown SiO_2 MOS capacitor is shown in figure 3.7. In this GV spectra, the well-known conductance peak appears near flatband condition which is due to the response from interface traps near the Fermi level [15]. Considering Figure 3.7 again we note a non-zero conductance when the sample is under strong accumulation bias. Under such bias conditions the Fermi level at the SiO_2/SiC interface is very close or even above the SiC conduction band edge. In the case of Si MOS capacitors the conductance signal is usually negligible in accumulation while here in SiC MOS capacitors, the conductance is non-zero and becomes constant at high accumulation bias. The conductance in accumulation increases with frequency and similar behavior can be observed if there is a high series resistance within the MOS capacitor [15]. This behavior in SiC MOS samples was normally attributed to series resistance and accumulation GV data was not investigated carefully. However, recent investigations report that this accumulation conductance signal stems not only from the series resistance but also from tunneling of electrons to and from NITs [81-83]. It turns out that we can estimate the density of NITs from accumulation GV data and this is discussed in papers B and E.

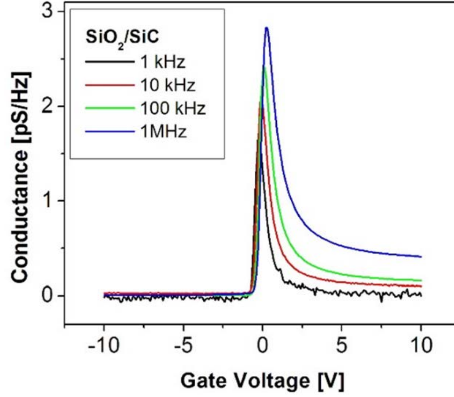


Figure 3.7 Room temperature GV spectra of a MOS sample with thermal SiO_2 grown in O_2 at four test signal frequencies between 1 kHz and 1 MHz.

A method to estimate the density of NITs and series resistance from such accumulation GV and CV data was first reported by Yuan et al [81,82]. In that so called distributed border traps model, the NITs are distributed throughout the oxide and their impact is calculated using an equivalent circuit model, shown in figure 3.8 (a), adding the incremental contributions of each trap to the total conductance and capacitance of the MOS capacitor. The admittance for given thickness of the dielectric is expressed as

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon} + \frac{j\omega q^2 N}{1+j\omega\tau e^{2kx}} \tag{3.4}$$

$$Y(x = dielectric\ thickness) = G_{tot} + j\omega C_{tot} \tag{3.5}$$

Here, G_{tot} and C_{tot} are total conductance and capacitance, k is the tunneling attenuation coefficient of the electron wavefunction with energy E, and can be written as

$$k = \sqrt{2m^*(E_{ox} - E)}/\hbar$$

where m^* is the electron effective mass and E_{ox} is the energy-barrier height for the tunneling. ε is the dielectric constant of the dielectric. τ is the interface trap response time and N is the volume density of NITs.

By fitting the experimental accumulation capacitance and conductance data as a function of frequency with simulated data using equation 3.4, we can determine the volume density of NITs. An example of experimental conductance data and the result of such a fitting procedure is shown in figure 3.8 (b).

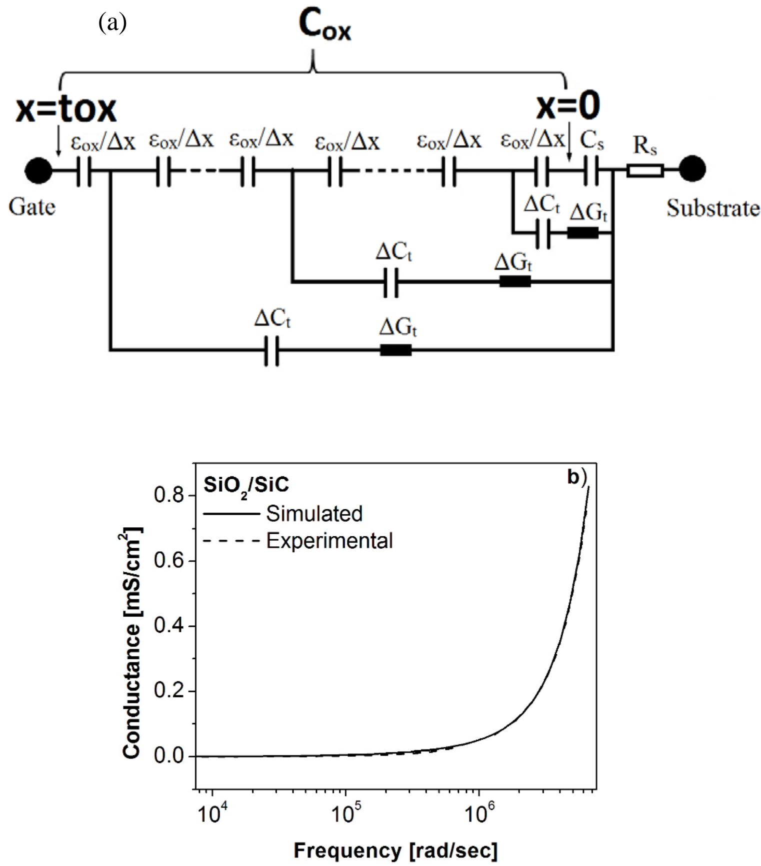


Figure 3.8 (a) Equivalent circuit of a MOS capacitor taking into consideration the presence of NITs. The capacitor is biased in strong accumulation. From [81]. (b) Simulated and experimental accumulation conductance data for a MOS sample with SiO_2 as dielectric.

Under the strong accumulation condition the series resistance, R_s, has a greater impact on the conductance than the capacitance. R_s can be extracted by plotting the experimental data in the accumulation region, $G_m/\omega C_m^2$, against frequency where C_m and G_m are the experimental capacitance and conductance at the accumulation voltage and ω is the angular frequency [82]. An example of such a plot is given in figure 3.9. Here the value of R_s is ~ 1×10^{-3} (Ω.cm^2).

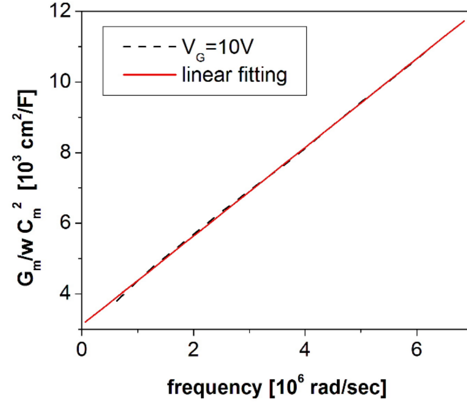


Figure 3.9 A plot of $G_m / (\omega C_m^2)$ against ω for extraction of series resistance.

3.2.4 Current-Voltage measurements

Current-voltage (IV) measurements are made to estimate the leakage current characteristics, the critical breakdown field and tunneling barrier height of the dielectric material. The breakdown field across the sole dielectric or stack of two or three different dielectrics e.g. dual dielectric stack of AlN with SiO_2 in the MOS capacitors, can be determined by the following expressions [84].

$$E = \frac{V_G - V_{FB}}{t_{ox}} \tag{3.6}$$

$$E_{eff} = \frac{V_G - V_{FB}}{t_{ox,total}} \tag{3.7}$$

$$E_{AlN} = \frac{V_G - V_{FB}}{t_{AlN}} \times \frac{C_{ox,SiO2}}{C_{ox,SiO2} + C_{ox,AlN}} \tag{3.8}$$

where V_G, V_{FB}, t_{ox} and C_{ox} are the gate voltage, flatband voltage, oxide thickness and oxide capacitance respectively. Equation 3.6 deals with sole dielectric MOS capacitors while the equations 3.7 and 3.8 concern stacked dielectrics. Equation 3.7 treats the stacked dielectrics as a single dielectric while equation 3.8 is used to find the electric field across the desired dielectric in a stack by considering the mismatch in the dielectric constants. Here equation 3.8 is an example of the electric field across AlN in a dual dielectric stack of AlN with SiO_2.

From the leakage current behavior, the tunneling barrier height of the dielectric materials can be determined by using the suitable tunneling mechanism. In our study, a Fowler-Nordheim (F-N) tunneling behavior is observed when examining the leakage current density vs electric field (J-E) profile of our MOS samples. An example is shown in figure 3.10. The tunneling barrier height of the dielectric material is extracted from analysis of the F-N tunneling where the current density across MOS devices at high fields is described by [85]:

$$J = AE^2\, exp\left(\frac{-B}{E}\right) \tag{3.9}$$

Where, $A = \frac{q^3 m}{8\pi h m_{ox}\phi_b}$ and $B = \frac{8\pi\sqrt{2m_{0x}}\,\phi_b^{\frac{3}{2}}}{3hq}$

The parameters A and B depend on the tunnel barrier height ϕ_b and the effective mass of the tunneling electron m_{ox} in the oxide. A and B can be determined from experimental IV characteristics plotted as $ln\ (J/E^2)$ vs. $1/E$, a so-called F-N plot. This is shown in figure 3.10 (b). The slope of the straight line gives B while A is determined from the intercept. Parameter B is the exponent in equation (3.9) for F-N tunneling current density and is the prominent parameter in determining the current flow in the gate dielectrics [83]. In figure 3.10 of our dry SiO_2 sample, the value of B taken from the slope of F-N plot at high electric field across the oxide is 175 MV/cm. The effective barrier height for the SiO_2 /4H-SiC interface extracted from this analysis is 2.50 eV by taking m_{ox} in SiO_2 to be $0.4m_0$ where m_0 is the free electron mass [86]. This barrier height is reasonably close to the previously reported values for dry SiO_2 determined by F-N tunneling mechanism [86].

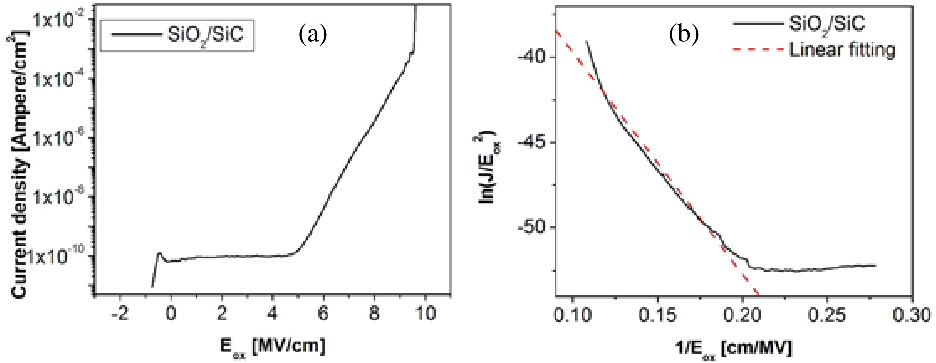


Figure 3.10 (a) Leakage current density versus electric field (J-E) of a SiO_2/SiC MOS sample. (b) Fowler-Nordheim plot for the same device.

4 Main results

4.1 Al_2O_3 as a gate dielectric in 4H-SiC MOS capacitors

This work is detailed in papers A and D. In this work, Al_2O_3 is used as a dielectric for MOS capacitors either as a single layer or in stack with SiO_2. Al_2O_3 is grown by different methods. We find that an Al_2O_3 layer grown by repeated deposition and subsequent low temperature (200°C) oxidation of thin Al layers using a hot plate contains significantly lower density of traps at the Al_2O_3/SiC interface compared to Al_2O_3 grown by other deposition methods. We refer to this sample as hot plate Al_2O_3. A comparison of the density of interface traps among differently grown Al_2O_3 along with reference dry thermal SiO_2 is demonstrated in figure 4.1. It is evident in the figure that the hot plate Al_2O_3 sample contains the lowest density of interface traps. The interface trap density in a stack of SiO_2/hot plate Al_2O_3 dielectric is comparable to reference thermally grown SiO_2 grown in N_2O ambient. The ALD grown Al_2O_3 has a peak in the interface state density about 0.45 eV below the SiC conduction band edge. The Al_2O_3 sample grown by RTP oxidation of Al contains very large amounts of interface traps.

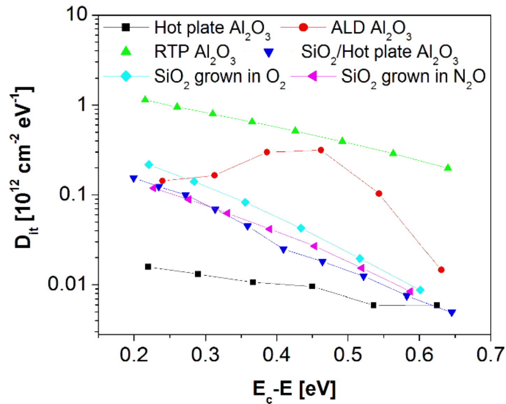


Figure 4.1 Density of interface states as a function of energy from the SiC conduction band edge for the sole and stack Al_2O_3 dielectric samples grown by different methods and reference samples with thermal SiO_2 grown in O_2 or N_2O ambient.

Electron injection into the Al_2O_3 dielectric during positive gate bias stress is observed. However, the release of the injected electrons by UV light exposure shows that the Al_2O_3 samples do not have significant negative fixed charge as frequently suggested in literature but rather trapped electrons. The capture and emission of electron from the traps within the Al_2O_3 gate dielectric is expressed in figure 4.2 which shows the effect of bias stress and UV light exposure on the CV curves of the MOS capacitor.

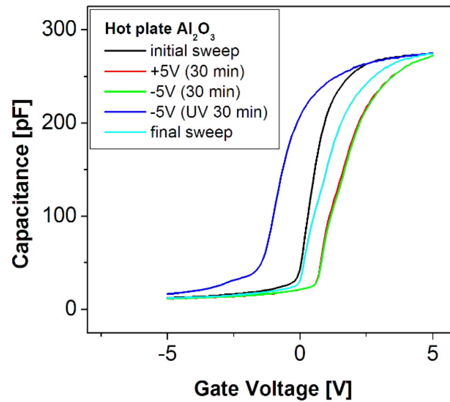


Figure 4.2 C-V characteristics (100 kHz) of a hot plate Al_2O_3 sample at room temperature before and after applying bias stress or UV illumination to it. The black curve denotes the first reference curve while the light blue curve is the final curve recorded at the end of the experiment.

In this figure 4.2, the first reference CV (black curve) sweep is taken by applying gate voltage from depletion to accumulation. The MOS capacitor is then kept in accumulation (+5 V) for 30 min and then the bias is swept from depletion (-5 V) to accumulation (+5V) and the CV (red curve) is recorded. Electrons are injected into the oxide during the accumulation bias stress and electron trapping is detected as a positive flatband shift. Next, a depletion bias of -5 V is applied for 30 min to examine if electrons are released from oxide traps under such conditions. The CV (green curve) is recorded directly thereafter and it is almost identical to the curve recorded after the accumulation bias stress CV (red curve) which shows that there is insignificant release of electrons from oxide traps under depletion condition. The sample is now kept under depletion bias and illuminated by UV light for 30 min. Thereafter, the UV light is turned off and a CV sweep is recorded from depletion towards accumulation (dark blue curve). A large negative flatband voltage shift is observed and it is evident that electrons trapped in the Al_2O_3 are released during the UV exposure. However, these traps are filled again once the sample is biased in accumulation as observed in the subsequent CV sweep (light blue curve). The CV curve shifts towards positive voltages and remains stable thereafter upon repeated measurements.

The possible effect of the UV light is twofold. First, it is possible that the UV photons are “absorbed” by the trapped electrons in the Al_2O_3 resulting in a release of the electrons to the SiC conduction band. Second, the UV exposure creates electron hole pairs and the depletion layer shrinks correspondingly. This means that the electric field across the oxide increases which can result in enhanced field assisted emission of electrons from traps within the Al_2O_3 to the SiC conduction band. We cannot distinguish between these two possibilities in this experiment.

IV measurements are made on the Al_2O_3 MOS samples to study the dielectric leakage properties. Leakage current density vs effective electric field (J-E) curves for our Al_2O_3 samples together with a sample containing thermally grown SiO_2 are shown in figure 4.3. The hot plate Al_2O_3 film has a breakdown field of ~ 5 MV/cm which is significantly higher than in the ALD and RTP Al_2O_3 films. This value of the breakdown field is about half the

breakdown field achieved in the reference SiO_2/SiC MOS capacitor (light blue curve). In case of an SiO_2/Al_2O_3 stack (dark blue curve), the effective breakdown field, considering the dual dielectric as a single dielectric, is ~ 8 MV/cm. A hard breakdown is observed in a stacked sample around 5 MV/cm but before that, the leakage current value is relative low ~ 10^{-8} A/cm. The electric field across the Al_2O_3 dielectric in the SiO_2/Al_2O_3 stack at the point of breakdown is determined by equation 3.8 and is ~ 5.5 MV/cm. This shows that the addition of the SiO_2 layer on top of the hot plate Al_2O_3 has not much impact on the breakdown field of Al_2O_3. However, the benefit of the stacked dielectrics MOS capacitor is that it can be operated at higher gate voltages. Fabrication of such a dielectric stack is needed in order to make Al_2O_3 a realistic alternative to SiO_2 as a gate dielectric in 4H-SiC MOS devices.

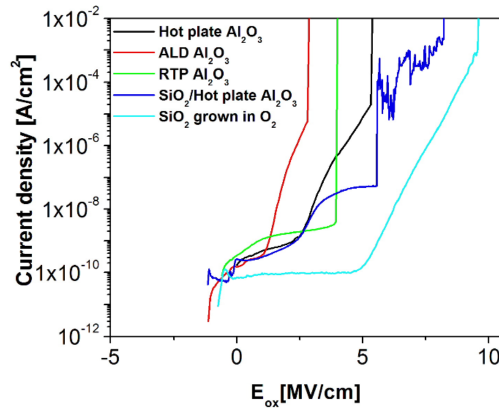


Figure 4.3 Comparison of leakage current density vs electric field across the dielectric (J-E) of differently prepared Al_2O_3 samples along with a reference sample with thermal SiO_2 grown in O_2.

4.2 AlN as a gate dielectric in 4H-SiC MOS capacitors

The details of this research are given in paper C. In this work, AlN dielectric is grown as a single crystal on n-type 4H-SiC samples by hot-wall MOCVD at high temperature (1100°C). Wide bandgap dielectrics such as Al_2O_3, SiO_2 or Si_3N_4 are deposited by different methods on top of the AlN layer to investigate their effect on the electrical quality of the AlN/SiC interface. Interface and near interface states density analysis demonstrate that a sole AlN layer grown on SiC results in an excellent AlN/SiC interface with extremely low density of interface traps. A comparison of the density of interface traps in differently prepared samples is shown in figure 4.4. It is evident that a single layer AlN sample has the lowest interface trap density while the interface density in the stacked dielectrics is somewhat higher but still much lower than in a reference SiO_2 sample (apart from the AlN/Si_3N_4 sample). So, the addition of different dielectric layers on the top of AlN has in general a negative but not lethal impact on the AlN/SiC interface quality.

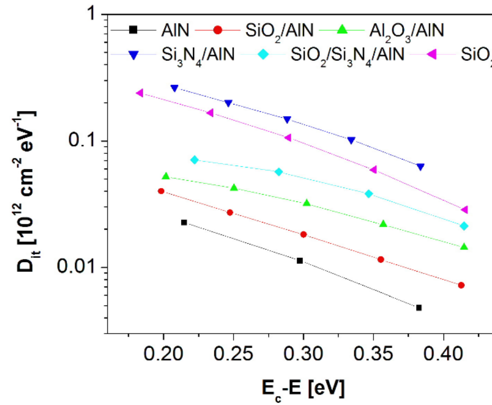


Figure 4.4 Density of interface states as a function of energy from the SiC conduction band edge for the sole and stack AlN dielectric samples with a thermally grown SiO_2 reference sample.

Electron injection into the AlN layer is observed when electrons are accumulated at the interface. This injection is reversible but causes large unwanted flatband voltage shift in the MOS structures. The emission of electrons from the traps within the AlN dielectric is investigated carefully. For this purpose, firstly the traps are intentionally filled with electrons at room temperature by biasing at 20 V for 10 minutes. The flatband voltage of a AlN MOS sample prior to accumulation bias stress was around 1 V and after the bias stress was noted to about 14 V. Afterward, the sample is kept at an elevated temperature and at depletion bias of 0 V for a certain time period. Then subsequent CV sweeps are made, to accumulation voltage of less than 20 V, to get an estimate of the rate of emission of electrons by monitoring the flatband voltage shift. This experiment is performed at three different temperatures of 320 K, 360 K and 400 K. The result of time and temperature dependent electron emission is shown in figure 4.5. This experiment demonstrates that the electrons trapped within the dielectric can be released to the SiC using a depletion bias and by raising the temperature of sample.

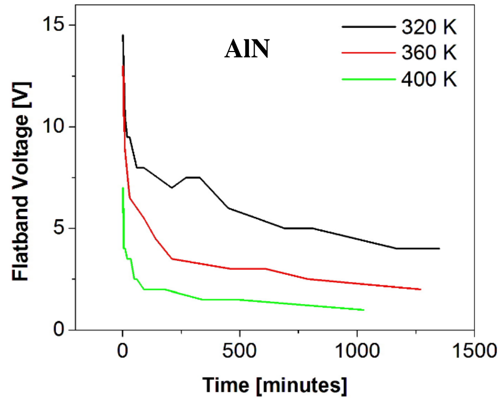


Figure 4.5 Observation of time and temperature dependent electron emission from traps within AlN dielectric by performing CV measurements subsequently at different time intervals for a given fixed temperature after first intentionally filling the traps with electrons. The flatband voltage value before the accumulation bias stress was 1 V and after the bias stress around 14 V.

The dielectric leakage properties are investigated using IV analysis. Leakage current density as a function of the effective electric field (J-E) is expressed in figure 4.6. The plot shows that the breakdown electric field across the sole AlN dielectric is about 3 MV/cm. A noticeable thing in the J-E profile is the current leakage behavior across the dielectric that is different in sole AlN and the stacked SiO_2/AlN MOS sample. An abrupt leakage is observed in the sole AlN MOS sample but not in the SiO_2/AlN stack. This indicates the wide bandgap dielectric on top of the AlN limits the current leakage across the AlN layer. It is evident that the addition of SiO_2 increases the breakdown field if the stack is taken as a single dielectric layer. However, if the field across the AlN layer within the stack at breakdown is calculated using equation 3.8 one obtains ~ 4 MV/cm which is a slight improvement compared to a single AlN layer. However, the benefit of using an additional SiO_2 layer is that such a MOS capacitor can tolerate higher gate voltages than a sole AlN layer. More studies on the dielectric stacks are needed to reveal if they can be an alternative to SiO_2 as a gate dielectric in 4H-SiC MOS devices.

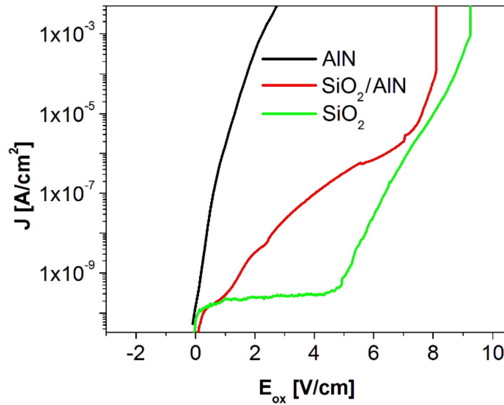


Figure 4.6 Comparison of leakage current density versus electric field for a single layer AlN MOS capacitor, a stack of SiO_2/AlN and dry thermal SiO_2 MOS capacitor.

A comparison of the density of interface states of different gate dielectrics grown on 4H-SiC is presented in figure 4.7. This figure shows that AlN has excellent interface quality with SiC compared to the SiO_2 and Al_2O_3 in terms of interface trap density. This makes AlN an attractive candidate as a gate dielectric in SiC MOS technology provided that the electron injection into the AlN as discussed above can be reduced significantly.

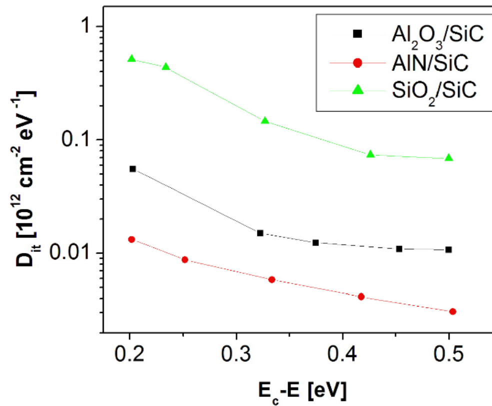


Figure 4.7 A comparison of the density of interface states (D_{it}) for Al_2O_3, AlN or SiO_2 gate dielectrics as a function of energy from the SiC conduction band edge.

4.3 Extraction of the density of near-interface traps (NITs) from a conductance signal in SiC MOS capacitors under strong accumulation

The details of this work are provided in papers B and E. We find a clear correlation between the density of near-interface traps (NITs) in MOS capacitors, fabricated on off-axis (0001) and on-axis (11$\bar{2}$0) face n-type 4H- and 6H-SiC with dry oxides, and the strength of a conductance signal observed under strong accumulation. The conductance signal strength in capacitors having dry thermal oxides varies with temperature and can be described by electron capture and emission at NITs at a rate close to the ac test signal frequency. The findings here show that the signal depends on temperature due to thermal emission of electrons from the NITs rather than direct tunneling. This is expressed in figure 4.8. However, direct tunneling is also present and is more prominent in samples containing low density of NITs such as oxides made by sodium enhanced oxidation (SEO). It is possible to estimate the density of NITs from the conductance data using models previously developed for studies of high-k dielectrics. The density of NITs determined by such a model for our investigated samples is close in magnitude to previously estimated values of NITs in identical samples using a technique called thermal dielectric relaxation current (TDRC) [34,88-90]. A comparison of the surface density of NITs (S_{bt}) extracted by the model and by the TDRC method is shown in table 4.1.

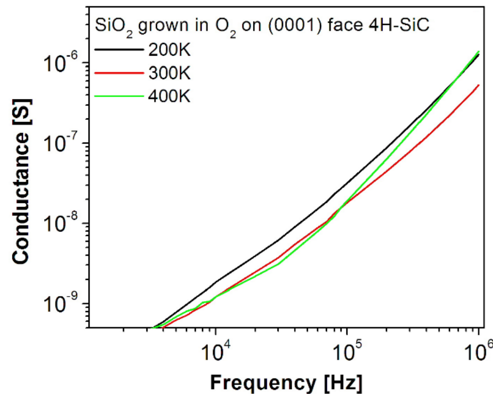


Figure 4.8. Conductance measured at a gate voltage of 9.5V over different frequencies and temperatures for a MOS sample with thermally grown SiO_2 grown in O_2 ambient.

Table 4.1. Comparison of surface density of NITs (S_{bt}) extracted by the model and by TDRC

SiC MOS device	S_{bt} by simulation model	S_{bt} by TDRC
(0001) faced 4H-SiC MOS device with oxide		
grown in O_2 ambient	~ $2x10^{12}$ cm^{-2}	~ $3x10^{12}$ cm^{-2}
grown in N_2O ambient	~ 5×10^{11} cm^{-2}	~ 1×10^{12} cm^{-2}
grown by SEO	~ 4×10^{10} cm^{-2}	~ 1×10^{11} cm^{-2}
(0001) faced 6H-SiC MOS device with oxide		
grown in O_2 ambient	~ 1×10^{11} cm^{-2}	~ 3×10^{11} cm^{-2}
$(11\bar{2}0)$ faced 4H-SiC MOS device with oxide		
grown in O_2 ambient	~ $1.5x10^{12}$ cm^{-2}	~ $2x10^{12}$ cm^{-2}

5 Conclusions and suggestions for future work

The CV analysis shows that Al_2O_3 and AlN have very good interface quality with SiC as compared to SiO_2 in terms of the density of interface states. The interface traps observed at the SiO_2/SiC interface are practically absent at the Al_2O_3/SiC and the AlN/SiC interfaces. The approaches to obtain the best dielectric properties when growing these materials on SiC are different. In the case of Al_2O_3, amorphous layers provide the best results which is mainly due to the large lattice mismatch between crystalline Al_2O_3 and 4H-SiC. This means that low deposition temperatures, preferably below 400°C, are needed to avoid partial crystallization of the Al_2O_3 which normally leads to excess leakage current paths through the grain boundaries. Among our Al_2O_3 samples, that are grown by different techniques, the so called hot plate grown Al_2O_3 shows the best overall results. The conclusion is that Al_2O_3 grown by repeated depositions and subsequent low temperature (200°C) oxidations of thin Al layers, using a hot plate, is in our case a better method than using atomic layer deposition (ALD).

In the case of growth of AlN on 4H-SiC it is possible to grow epitaxial AlN single crystalline thin films directly on the 4H-SiC because of the small lattice mismatch (1%). Here we grow such layers by MOCVD at 1100°C and this method provides excellent AlN/SiC interfaces virtually free from interface states.

In both the case of Al_2O_3 and AlN dielectrics, severe electron trapping is observed when electrons are accumulated at the dielectric/SiC interface. The electrons are apparently injected into the dielectric and reside some distance away from the interface. The trapped electrons act as an effective fixed charge within the dielectric resulting in a positive flatband voltage shift in the MOS capacitors. But these electrons can be released by applying depletion bias stress in combination with either UV light exposure or by raising the temperature. The presence of fixed negative charge in Al_2O_3 and AlN layers is frequently reported in the literature without any experiments being made to reveal the immobility of such charge. Our experiments reveal that mobile electrons rather than fixed negative charges are present in our Al_2O_3 and AlN dielectrics. In order to be able to use AlN or Al_2O_3 as a gate dielectric this electron injection needs to be suppressed significantly.

IV measurements of our MOS devices indicate that the MOS devices with Al_2O_3 or AlN as a gate dielectric have rather low breakdown fields i.e. ~ 5 MV/cm or ~ 4 MV/cm respectively. These values are about half the breakdown field obtained using thermal SiO_2. We demonstrate that it is possible to increase the breakdown voltage of the MOS capacitor by adding a wide bandgap dielectric layer on top of Al_2O_3 or AlN. The best candidate there is SiO_2. Extraction of the breakdown field across such dielectric stacks reveals that the breakdown field across the Al_2O_3 or AlN layers remains more or less unchanged but the additional SiO_2 layer increases the breakdown voltage of the MOS device. Furthermore, CV measurements show that by using a stack of Al_2O_3 or AlN with SiO_2 it is still possible to obtain Al_2O_3/SiC and AlN/SiC interfaces with low interface state densities.

The rather low breakdown field and electron trapping within the Al_2O_3 and AlN dielectrics is an issue when realizing n-channel MOSFETs. These challenges can possibly by tackled by depositing a thick SiO_2 layer on the top of an extremely thin (2-3 nm) AlN or Al_2O_3 dielectric. For future work, we would like to process n-channel MOSFETs with AlN or Al_2O_3 as a gate dielectric after solving the encountered challenges of electron trapping within the dielectrics.

In GV analysis, a non-zero accumulation conductance and frequency dispersion is observed for SiC MOS capacitors. This behavior in SiC MOS samples was normally attributed to series resistance and not carefully investigated. Haasmann et al [87] proposed that this non-zero accumulation conductance signal stems from tunneling of electrons to and from NITs rather than the series resistance and the signals strength is independent of temperature but they did not quantify the density of NITs. Our investigations show that the strength of conductance signal and frequency dispersion in the accumulation region of GV curves is a combination of a response from NITs and the series resistance of the sample. Furthermore, we find that the signal strength is in general temperature dependent due to thermally activated capture of electrons in NITs. Moreover, we calculated the density of the NITs by using distributed border traps model proposed by Yuan et al [81] and the results are in agreement with estimates of NITs using other methods such as thermal dielectric relaxations transients (TDRC). We conclude that this conductance method is a quick method that can be used at room temperature to obtain a first order estimate of NITs in differently prepared oxides.

6 Summary of appended papers

This chapter presents a brief summary of the content of the appended papers and a short description of my contribution to each paper.

Paper A

Low density of near-interface traps at the Al_2O_3/4H-SiC interface with Al_2O_3 made by low temperature oxidation of Al

In this paper, Al_2O_3 is used as a dielectric for n-type 4H-SiC MOS devices. Al_2O_3 was grown by low temperature growth methods such as thermal oxidation of thin Al layers and atomic layer deposition (ALD). The interface and near interface traps are studied in detail at the Al_2O_3/SiC interface by using CV techniques at different temperatures. The CV results demonstrate that Al_2O_3 grown by thermal oxidation of Al has very good interface properties when grown on n-type 4H-SiC. A breakdown field of ~5 MV/cm is observed for the Al_2O_3 layers.

My contributions: performed electrical characterization of the Al_2O_3/SiC interface and wrote the paper.

Paper B

Conductance signal from near-interface traps in n-type 4H-SiC MOS capacitors under strong accumulation

In this paper, thermally grown dry oxides and oxides made by sodium enhanced oxidation (SEO) are investigated as gate dielectrics for n-type 4H-SiC MOS devices. The GV technique is used to study NITs in these samples. It is observed that the conductance signal in n-type 4H-SiC MOS capacitors in accumulation can be described by tunneling of electrons between NITs and the SiC conduction band. It is also seen that the response of NITs to free carriers is partially temperature dependent.

My contributions: Did electrical analysis, performed modeling to quantify the density of NITs and wrote the paper.

Paper C

Electrical properties of 4H-SiC MOS capacitors with AlN gate dielectric grown by MOCVD

In this paper, AlN is used as a dielectric either a sole or in stack with different dielectrics like SiO_2, Al_2O_3 or Si_3N_4 for n-type 4H-SiC MOS devices. Interface quality of MOCVD grown AlN/SiC interfaces are investigated by using different electrical characterization techniques like CV, GV or IV. We find that a high quality AlN can be grown by MOCVD on 4H-SiC. A low breakdown field and trapping of free electrons deep inside AlN is observed. A dielectric stack consisting of a top layer of deposited SiO_2 and a bottom layer

of AlN on SiC has higher breakdown voltage than a single layer of AlN and maintains low density of interface states at the AlN/SiC interface.

My contributions: Performed electrical characterization and wrote the paper.

Paper D

Electrical characterization of amorphous Al_2O_3 dielectric films on n-type 4H-SiC

In this paper, low temperature grown Al_2O_3 is used as a dielectric either a sole or in stack with SiO_2 for n-type 4H-SiC MOS devices. Al_2O_3 is grown by thermal oxidation of Al, ALD or RTP. Interface quality of Al_2O_3/SiC interface is investigated using different electrical characterization techniques such as CV, GV and IV. We find that Al_2O_3 films grown by low temperature growth methods have good interface quality with 4H-SiC. A breakdown field of 5MV/cm is observed and considerable reversible trapping of free electrons is observed within the Al_2O_3 layer. A dielectric stack of PECVD grown SiO_2 on the top of Al_2O_3 results in a structure with higher breakdown voltage while maintaining a good quality Al_2O_3/SiC interface.

My contributions: Performed electrical characterization and wrote the paper.

Paper E

Study of near-interface traps in n-type 4H-SiC MOS capacitors from conductance signal under strong accumulation

In this paper, dry SiO_2 is grown on off-axis (0001) and on-axis $(11\underline{2}0)$ face n-type 4H- and 6H-SiC to study the NITs using the accumulation conductance method. We find a correlation between the density of NITs and the strength of a conductance signal observed under strong accumulation. The strength of accumulation conductance signal varies with temperature due to thermal emission of electrons from the NITs. However, a temperature independent behavior is also observed in samples containing low density of NITs.

My contributions: Investigated the NITs by using GV characterization techniques. Quantified the density of NITs by modeling and wrote the paper.

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Included Publications

Paper A

Low density of near-interface traps at the Al_2O_3/4H-SiC interface with Al_2O_3 made by low temperature oxidation of Al

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*Materials Science Forum, **897**, 135-138 (2017).*

Materials Science Forum
ISSN: 1662-9760, Vol. 897, pp 135-138
doi:10.4028/www.scientific.net/MSF.897.135
© 2017 Trans Tech Publications, Switzerland
Submitted: 2016-09-18
Revised: 2016-12-31
Accepted: 2017-01-27

Low Density of Near-Interface Traps at the Al_2O_3/4H-SiC Interface with Al_2O_3 Made by Low Temperature Oxidation of Al

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Keywords: Interface states, Near-interface traps, Gate dielectrics, Aluminum oxide

Abstract. We report on a very low density ($<5\times10^{11}$ cm^{-2}) of near-interface traps (NITs) at the Al_2O_3/4H-SiC interface estimated from capacitance-voltage (CV) analysis of MOS capacitors. The aluminum oxide (Al_2O_3) is grown by repeated deposition and subsequent low temperature (200 °C) oxidation for 5 min of thin (1-2 nm) Al layers using a hot plate. We refer to this simple method as hot plate Al_2O_3. It is observed that the density of NITs is significantly lower in the hot plate Al_2O_3 samples than in samples with Al_2O_3 grown by atomic layer deposition (ALD) at 300 °C and in reference samples with thermally grown silicon dioxide grown in O_2 or N_2O ambient.

Introduction

Recently, 4H-SiC metal-oxide semiconductor field-effect transistors (MOSFETs) have emerged on the market for high voltage (> 900 V) applications [1, 2]. Lower voltage devices (400 – 600 V) are still hampered by the low inversion channel mobility which stems to a large degree from relatively high density of near-interface traps (NITs) at the SiO_2/SiC interface. Currently thermal oxides grown or annealed in NO (or N_2O) ambient are the mainstream dielectrics but more reduction in NITs is needed [3]. The main focus has been on thermal SiO_2 even though other oxides e.g. Al_2O_3 and HfO_2 have also been investigated [4-7]. While HfO_2 is a promising gate oxide material for Si, it is not suitable for SiC MOS devices because of the low conduction band offset at the HfO_2/4H-SiC interface [7, 8].

Al_2O_3 grown by atomic layer deposition (ALD) on SiC typically contains high density ($\sim1\times10^{13}$ cm^{-2}) of negative fixed charges that cause a shift of flat band voltage of MOS devices. This charge is reduced after annealing at 1000^0C but the Al_2O_3/SiC interface then contains high density of interface traps [4]. Recently, Al_2O_3 films grown by ALD and by low temperature oxidation of a thin Al layer have been used as gate dielectrics in graphene field effect transistors [9, 10]. The structure and morphology of Al_2O_3 made by oxidation of Al has been investigated with respect to the oxidation temperature. For temperatures below 300 ºC a uniform amorphous Al_2O_3 film forms while at higher oxidation temperatures a non-uniform amorphous Al_2O_3 film initially develops that gradually transforms into crystalline γ-Al_2O_3 [11].

In this work we investigate the interface quality of aluminum oxides made by ALD and by low temperature oxidation of Al. We find that it is possible to grow Al_2O_3 films with low density ($<1\times10^{12}$ cm^{-2}) of fixed negative charge and low density of NITs at the Al_2O_3/4H-SiC interface.

Experimental Methods

In our study, Al_2O_3 layer is formed by deposition of 1-2 nm thick Al layer on SiC substrate. The samples are first etched in HF and then directly transported into a vacuum chamber where e-beam evaporation of Al is made at a rate of 0.5 A/s. Thereafter the samples are baked on a hot plate at a temperature of 200 °C for 5 minutes to form the Al_2O_3 layer. This process of deposition and subsequent oxidation is repeated twelve times to get target thickness of ~ 15nm with an overall time span of about 4 hours. Another Al_2O_3 layer is grown by atomic layer deposition (ALD) at 300 °C via thermal decomposition of $Al_2(CH_3)_6$ in water ambient. Circular MOS capacitors were then made using Al as a gate metal and the interface quality of these oxides with 4H-SiC were characterized by CV analysis using Agilent E4980A LCR meter. Reference MOS capacitors with thermal SiO_2 grown in dry oxygen and N_2O ambient were also analyzed.

Commonly, interface traps are classified into fast interface traps that are located exactly at the oxide/SiC interface and near-interface traps (NITs) that are located some distance (1-2 nm) inside the oxide. The fast interface states capture electrons rapidly and their density (D_{it}) is estimated here by conventional CV made at different frequencies ranging from 1 kHz to 1 MHz in the temperature range 100 – 350 K. However, the density of NITs is usually underestimated in such conventional CV analysis. There are two reasons for this, firstly a portion of the NIT are slow traps and are unable to respond to the test signal in conventional CV. Secondly their electron capture rate is too low lower than that of the fast interface states and the density of trapped electrons in NITs depends strongly on the field across the oxide. Therefore, the density of NITs is estimated here using CV analysis where the sample is cooled from room temperature to 77 K while keeping a certain accumulation (charging) voltage on the gate. The NITs are filled under strong accumulation which is detected as a positive flat band voltage shift during subsequent CV measurement at 77 K [12].

Results and Discussion

The room temperature CV curves at test frequencies of 1 kHz and 1 MHz of a hot plate Al_2O_3 sample are shown in Fig. 1. The Al_2O_3 layer has a thickness of 15 nm, as determined by X-ray reflectivity, and the dielectric constant deduced from the capacitance in accumulation is ~ 6.5. The negative fixed charges frequently observed within the Al_2O_3 are not present [4]. Oxide breakdown occurs around gate voltage of 8 V corresponding to an electric field strength of 5 MV/cm as shown in Fig. 2. A first estimate of the interface state density is extracted from frequency dispersion of the CV curves. In the case of hot plate Al_2O_3 such dispersion is hardly visible indicating a rather low interface state density. This is further revealed in Fig. 3 which shows the interface trap density extracted from CV dispersion data, in the temperature range 100 – 350 K, in several samples with differently prepared dielectrics. It is evident that the hot plate oxide sample contains the lowest density of interface traps.

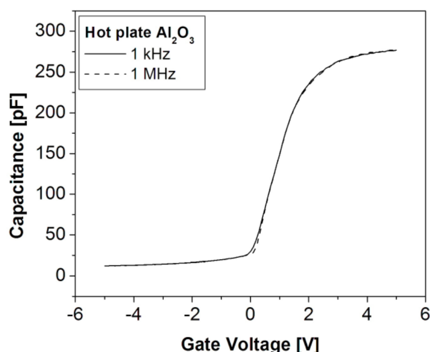

Figure 1. C-V curves of hot plate aluminum oxide capacitor at room temperature.

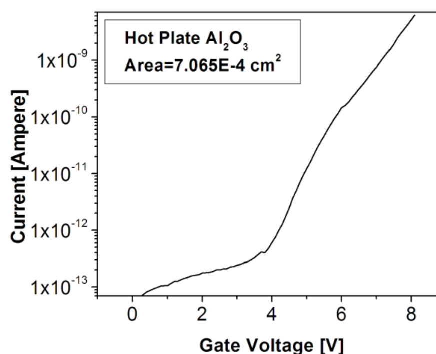

Figure 2. I-V curves of hot plate aluminum oxide capacitor at room temperature.

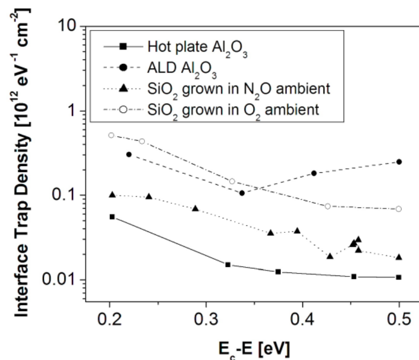

Figure 3. Interface state density as a function of energy from the SiC conduction band edge for differently prepared MOS capacitors. The data is extracted from hi_{1MHz}-low_{1kHz} CV measurements at different temperatures (100 – 350 K).

For comparison, MOSFETs using the reference N_2O grown oxide have field effect mobility of 25 cm^2/Vs [13].

The density of NITs is usually underestimated in the CV dispersion analysis as displayed in Fig. 3 (left). However, an estimate of the charge trapped in NITs can be obtained from CV analysis when the sample is cooled from room temperature down to 77 K while maintaining a certain charging voltage on the gate. The NITs are filled under strong accumulation and the density of trapped electrons increases with increasing accumulation bias. If the sample is cooled to 77 K with accumulation bias most of the captured electrons remain trapped in the NITs and then give rise to a positive flat band voltage shift during subsequent CV measurement at 77 K [12]. NITs density is then determined by using the expression NITs=C_{ox} $(V_{FB(G)}-V_{FB(GO)})/qA$ where $V_{FB(G)}$ and $V_{FB(GO)}$ are flat band voltages at different charging voltage and at zero voltage respectively.

An example of such analysis is shown in Fig. 4a for reference sample with SiO_2 grown in O_2 ambient and in Fig. 4b for hot plate Al_2O_3. In Fig.4a of the SiO_2 sample, a positive flat band shift is noted between the 77 K curves when the accumulation bias during cooling is increased. This shift is due to electron trapping in NITs during cool down under the influence of the electric field [12]. This shift is approximately 4 V when the accumulation bias is raised from 0 to 5 V. A ledge is seen at CV curve of SiO_2 sample at charging voltage of 0 V which indicates the presence of deep traps that were empty at zero charging voltage. While electron trapping is very different in the hotplate Al_2O_3 as shown in Fig. 4b. No pronounced positive flat band voltage shift is obtained between the 77 K curves when the accumulation bias is increased during cooling. This means that the hot plate Al_2O_3 sample has insignificant trapping of electrons in NITs.

The result of such analysis, showing the number density of electrons stored in NITs as function of the electric field across the oxide, for samples with differently prepared dielectrics is expressed in Fig. 5. The amount of electrons that are captured at the hot plate Al_2O_3/SiC interface is much lower than at the ALD Al_2O_3/SiC and thermally grown SiO_2/SiC interfaces. These results are rather remarkable and show that Al_2O_3 grown at low temperatures can result in a very low density of interface states at the Al_2O_3/SiC interface.

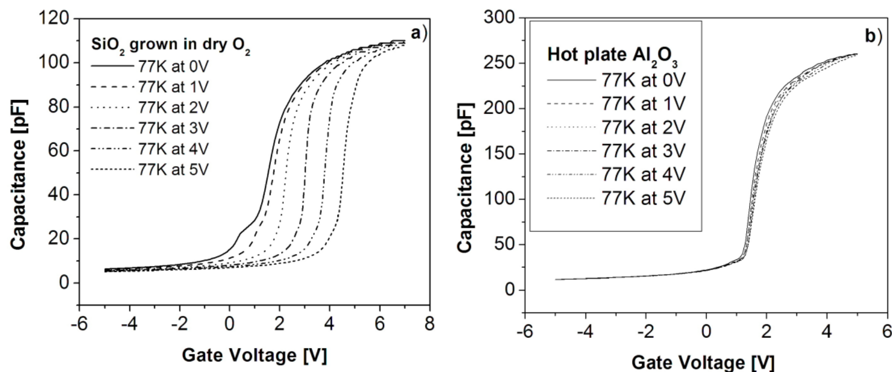

Figure 4. C-V measurements on (a) reference sample with SiO_2 grown in O_2 ambient and (b) low temperature Al_2O_3 at different charging bias (0 -5V) during cooling down to 77 K.

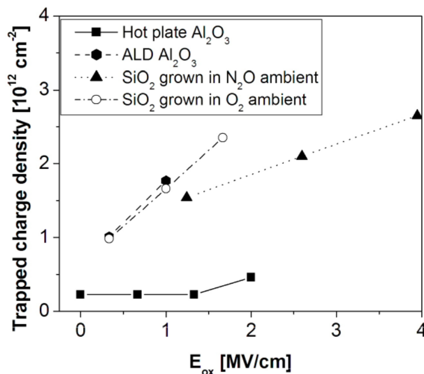

Figure 5. Number density of electrons trapped in interface states as a function of the electric field across the gate oxide during charging.

Conclusions

The hot plate Al_2O_3 has surprisingly good interface properties when grown on 4H-SiC. The near-interface traps (NITs) observed at the SiO_2/SiC interface are practically absent at the hot plate Al_2O_3/SiC interface. Furthermore, the hot plate Al_2O_3/SiC interface has low density ($<1\times10^{11}$ $eV^{-1}cm^{-2}$) of fast interface traps as compared to reference samples. Fixed negative charge has been a problem for ALD grown Al_2O_3 but such charge is practically absent within the hot plate Al_2O_3. However, the breakdown field of the Al_2O_3 is ~5 MV/cm and this is only about half the breakdown field achieved when using thermally grown SiO_2 as a gate dielectric. Further studies are needed to examine the possibility of improving the breakdown field strength without having negative impact on the interface properties.

Acknowledgements

This work was financially supported by The University of Iceland Research Fund. We also acknowledge support from the Swedish Foundation for Strategic Research (SSF), and the Knut and Alice Wallenberg Foundation (KAW).

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Paper B

Conductance signal from near-interface traps in n-type 4H-SiC MOS capacitors under strong accumulation

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*Materials Science Forum, **897**, 147-150 (2017).*

Materials Science Forum
ISSN: 1662-9760, Vol. 897, pp 147-150
doi:10.4028/www.scientific.net/MSF.897.147
© 2017 Trans Tech Publications, Switzerland
Submitted: 2016-09-19
Revised: 2017-01-02
Accepted: 2017-01-23

Conductance Signal from Near-Interface Traps in n-Type 4H-SiC MOS Capacitors under Strong Accumulation

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Keywords: Near-interface traps (NITs), Conductance analysis, Interfaces

Abstract. We find a clear correlation between the density of near-interface traps (NITs) in n-type 4H-SiC MOS capacitors and the strength of a conductance signal observed under strong accumulation. The conductance signal strength can be described by tunneling of electrons between the SiC conduction band and NITs at a rate close to the ac test signal frequency. The findings here show that the signal in dry thermal oxides depends on temperature which suggests that the electron capture cross section of the NITs is thermally activated. Direct tunneling is more prominent in samples containing low density of NITs such as oxides made by sodium enhanced oxidation (SEO).

Introduction

The low channel mobility of electrons in 4H-SiC MOSFETs stems from a large density of interface traps located at the SiC/SiO_2 interface [1]. The interface traps are commonly classified into fast interface traps that are located exactly at the oxide/SiC interface and near-interface traps (NITs) or border traps that are located some distance (1-3 nm) inside the oxide. Capacitance and conductance measurements are routinely used for characterization of insulator/semiconductor interfaces and the extraction methods are very well established [2]. One feature that is frequently observed in SiC MOS capacitors is a non-zero conductance when the sample is under strong accumulation bias. The conductance in accumulation increases with frequency and similar behavior can be observed if there is a high series resistance within the MOS capacitor [2]. This behavior in SiC MOS samples was normally attributed to series resistance and not carefully investigated. However, it was recently reported that this conductance signal stems from tunneling of electrons to and from NITs rather than the series resistance [3]. In this work we examine the conductance signal for several types of thermally grown oxides and investigate its correlation with NITs.

Experimental Methods

The silicon dioxide was thermally grown on n-type 4H-SiC either in dry oxygen ambient (oxide thickness 50 nm) or in the presence of intentional sodium contamination at a temperature of 1240°C (oxide thickness 100 nm). The method of oxide growth by intentional sodium contamination is often called sodium enhanced oxidation, SEO [4]. Circular MOS capacitors were then made using Al as a gate metal. To study the nature of interface traps of 4H-SiC MOS capacitors at different test frequencies, ranging from 1 kHz to 1 MHz, and at different temperatures, 100 K to 400 K, C-V and G-V measurements are performed by using an Agilent E4980A LCR meter.

Results and Discussion

The room temperature C-V and G-V curves, at test frequencies of 1 kHz and 1 MHz, of an n-type 4H-SiC MOS capacitor with thermal dry SiO2 are shown in Fig. 1. The C-V curves are typical for dry oxide samples showing some frequency dispersion due to interface traps near flatband (~ 0 V) and all the curves coincide at strong accumulation bias (10 V). In the G-V curves, Fig.1b, the well-known conductance peak occurs near flatband conditions and is due to response

from interface traps near the Fermi level [2]. The interesting feature here is the non-zero conductance when the sample is under strong accumulation bias. Under such bias conditions the Fermi level at the SiO_2/SiC interface is very close or even above the SiC conduction band edge depending on the density of NITs that can pin the Fermi level. In the case of Si MOS capacitors the conductance signal is usually negligible in accumulation while here the conductance is non-zero and becomes constant at high accumulation bias. The conductance in accumulation increases with frequency and similar behavior can be observed if there is a high series resistance within the MOS capacitor [3]. This behavior in SiC MOS samples was normally attributed to series resistance and not carefully investigated. However, it was recently reported that this conductance signal stems from tunneling of electrons to and from NITs rather than the series resistance [3]. We find that it is not possible to find a value for the series resistance that can explain the non-zero conductance in Fig.1 using the well-known method for such correction [2]. The same applies to all other SiC capacitors that we have investigated so our findings agree with ref. [3] with respect to series resistance. However, the series resistance has a certain impact on the high frequency data (above 100 kHz) as discussed below.

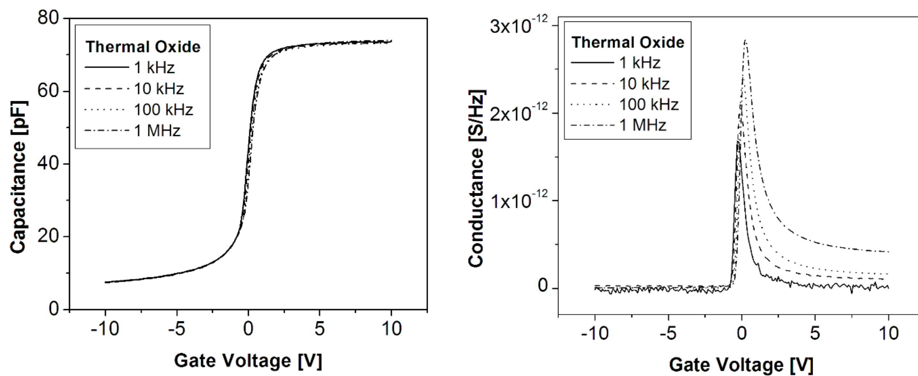

Fig.1 Room temperature a) C-V and b) G-V curves at different frequencies of n-type 4H-SiC MOS capacitor with thermally grown dry SiO_2.

Figure 2 shows the typical effect of temperature on the G-V curves for capacitors containing dry oxides. The conductance in strong accumulation (10 V) depends on the sample temperature and is in this case maximized at 200K. In ref [3] no temperature dependence was observed and the signal was therefore attributed to direct tunneling of electrons between NITs and the SiC conduction band. In our studies we note that the conductance signal exists at all temperatures (between 100-400 K) which supports the direct tunneling hypothesis. However, in addition there is a temperature dependent contribution to the signal that indicates thermally activated capture of electrons at the NITs. This is not a surprising result since it well established that NITs located near the SiC conduction band edge exhibit thermally activated electron capture with very wide range of electron capture cross sections [5,6].

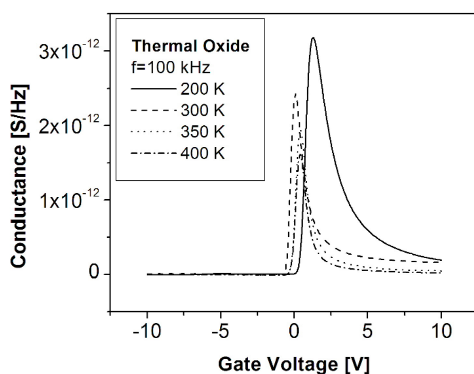

Fig.2 G-V curves at 100 kHz of SiO_2 grown in O2 at different temperatures.

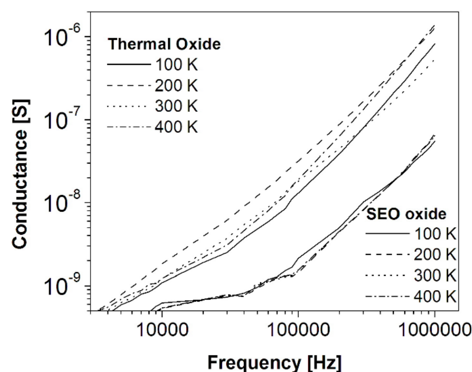

Fig.3 Conductance in accumulation (at gate voltage of 9.5 V) as a function of frequency and temperature for dry thermal oxide and an oxide made by sodium enhanced oxidation (SEO).

Figure 3 shows the accumulation conductance at a gate bias of 9.5 V of a dry oxide sample as a function of frequency and temperature. The same type of data is also shown for an SEO sample. The density of NITs in SEO oxides is an order of magnitude lower than in conventional dry oxides [4]. We see that the accumulation conductance signal in the SEO sample is about an order of magnitude lower than in the dry oxide sample. This strongly suggests that the signal scales with the density of NITs. It should also be noted that the conductance signal in the SEO sample does not vary significantly with temperature which suggest that it originates mainly from direct tunneling as in Ref. [3]. We expect that thermal oxides grown or annealed in NO ambient will behave in a similar manner as the SEO oxide.

NITs (or border traps) have been investigated intensively in high-k dielectrics grown on III-V semiconductors [8-10]. Direct tunneling and temperature dependent capture/emission from NITs has been observed [10]. The NITs in Al2O3 grown on InGaAs are known to have an impact on the accumulation conductance in G-V analysis as well as on the accumulation capacitance in C-V studies [8-9]. A method to estimate the density of NITs from such G-V and C-V data was reported in Ref. [8]. In that model the NITs are distributed throughout the oxide and their impact is calculated using an equivalent circuit model adding the incremental contributions of each trap to the total conductance and capacitance of the MOS capacitor. This model has been extended further to obtain the concentration depth profiles of NITs within the oxide as well as their location in energy [10]. We have used the model in Ref. [8] to estimate the density of NITs based on the conductance data in accumulation, taking also into account the possible effect of series resistance [9]. In the simulations presented here the energy level of the NITs is assumed to be at the Fermi level position but this simplification does not have a significant impact on the overall result. An example of the results of such a fitting procedure is shown in Figure 4 for an SEO oxide. The key fitting parameters are the density of NITs and the series resistance. The series resistance has an impact only at frequencies above 100 kHz in agreement with Ref. [9] as shown in Figure 5 for the dry oxide sample. The extracted active volume density of NITs at room temperature is ~ 8×10^{18} cm^{-3} in dry oxides and ~ 3×10^{17} cm^{-3} in SEO oxides. Using the methods developed in Ref. [10] the active depth of the NITs is of the order of 2 nm. This gives the surface density of NITs in the $2x10^{12}$ cm^{-2} range for dry oxides and $6x10^{10}$ cm^{-2} for the SEO oxide. These values are of the same magnitude as previous estimates of NITs in identical samples using thermal dielectric relaxation current (TDRC) [4]. More simulations are needed to test this model further, including the effect of temperature, but it provides an estimate of NITs which is in agreement with more elaborate experimental methods.

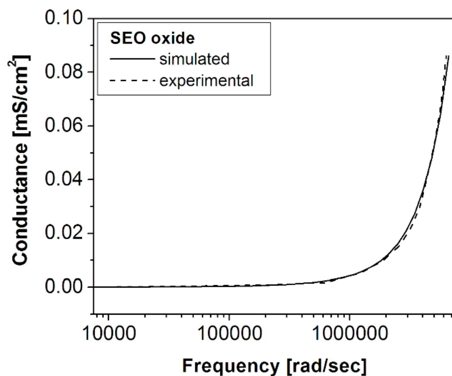

Fig.4. Simulated and room temperature experimental conductance data for SEO grown SiO_2 at gate voltage of 9.5V. The extracted volume density of NITs is $3x10^{17}$ cm^{-3} and the series resistance is $2.2x10^{-4}$ Ω cm^2.

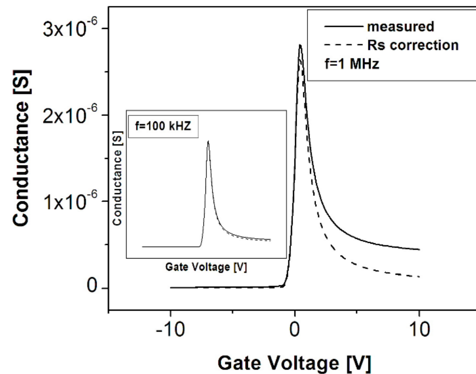

Fig.5. Series resistance (R_s) corrected G-V profile of thermal dry oxide at 1 MHz. R_s has very little impact on G-V curve at 100 kHz as shown in the inset. R_s is $1x10^{-3}$ Ω cm^2.

Conclusions

We find that the conductance signal in n-type 4H-SiC MOS capacitors in accumulation can be explained by tunneling of electrons between NITs and the SiC conduction band. It is possible to estimate the density of NITs from the conductance data using models previously developed for studies of high-k dielectrics [8-10]. Further studies of these conductance signals are needed to verify the usefulness of this approach to investigate NITs.

Acknowledgement

This work was financially supported by The University of Iceland Research Fund.

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Paper C

Electrical properties of 4H-SiC MOS Capacitors with AlN gate dielectric grown by MOCVD

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manuscript submitted for publication.

Electrical properties of SiC MOS Capacitors with AlN gate dielectric grown by MOCVD

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Abstract

We report on the electrical properties of the AlN/4H-SiC interface using capacitance- and conductance-voltage (CV and GV) analysis of AlN/SiC MOS capacitors. The crystalline AlN layers are made by hot wall MOCVD at 1100°C. CV analysis at room temperature reveals an order of magnitude lower density of interface traps at the AlN/SiC interface than at nitrided SiO_2/SiC interfaces. The density of near interface traps (NITs) estimated using conductance analysis in accumulation is comparable to a thermal oxide grown in N_2O. Electron trapping within the AlN is significant when the MOS capacitors are biased into accumulation resulting in a large flatband voltage shift towards higher gate voltage. This process is reversible and the electrons are fully released from the AlN layer if depletion bias is applied at elevated temperatures. Current-voltage (IV) analysis reveals that the breakdown electric field across the AlN dielectric is 3-4 MV/cm and a tunneling barrier height of 1.6 eV is deduced based on Fowler-Nordheim (F-N) mechanism. By depositing an additional SiO_2 layer on top of the AlN layer, it is possible to increase the breakdown voltage of the MOS capacitors significantly without having much impact on the quality of the AlN/SiC interface.

Introduction

4H-Silicon carbide (SiC) can be thermally oxidized to yield its native silicon dioxide (SiO_2) over its surface but the drawback is a rather poor interface quality of the SiO_2/SiC interface. This results in a low electron channel mobility in 4H-SiC MOSFETs due to electron trapping and scattering at the interface. The quality of the SiO_2/SiC interface has been improved by various oxidation and nitridation methods which has enabled the commercialization of the high voltage (> 900V) MOSFETs [1-3]. These high voltage devices can tolerate lower mobilities than the low voltage ones because the current is limited by the resistance of the low doped SiC used in these devices. However, for low voltage devices a further reduction in the interface state density near the SiC conduction band is needed to achieve an acceptable electron channel mobility. In an attempt to

overcome this various high-*k* gate dielectrics (e.g. Al_2O_3, HfO_2, AlN) are being explored for SiC MOS technology [4-12]. The large bandgap (~ 6.2 eV) AlN is a potential substitute for SiO_2 in SiC MOS devices [13-15]. The lattice mismatch between SiC and AlN is less than 1%, which enables a single crystalline growth of AlN films on SiC substrates [16]. AlN has been investigated on 4H-SiC and the reported conduction and valence band offsets are 1.7 eV and 1.3 eV respectively as determined by X-ray photoelectron spectroscopy (XPS) [17]. SiC MOSFETs with crystalline AlN as a gate dielectric grown by molecular beam epitaxy (MBE) have been reported but the structures were leaky and the channel mobility was very low (< 1 cm^2/Vs) [10,18]. Fixed charge and interface traps were observed in crystalline AlN grown by metal organic chemical vapor deposition (MOCVD) on 4H- and 6H-SiC [8,16]. Pre-irradiation of atomic nitrogen before growth and a flow of ammonia during ramp-up have been used to improve the quality of AlN film [8,19]. There is one report on the introduction of a thin SiO_2 layer between SiC and AlN as an additional barrier to prevent electron injection from the semiconductor to the dielectric [20].

In this study, we grow crystalline AlN by hot wall MOCVD on n-type 4H-SiC. In addition, we investigate the effect of adding wide bandgap dielectrics on top of the AlN layer. The interface and near-interface traps (NITs) at the AlN/4H-SiC interface are investigated by capacitance- and conductance-voltage (CV and GV) measurements on MOS capacitors. The dielectric breakdown properties are extracted from current-voltage (IV) measurements. We find that the AlN/4H-SiC interface contains very low density of interface traps and the detrimental traps observed at the SiO_2/4H-SiC interface are practically absent at the AlN/4H-SiC interface.

Experimental Methods

The SiC MOS samples used in this study have 10 µm thick n-type epitaxial layers with a net doping concentration of ~ 1×10^{16} cm^{-3} grown on 4 degrees off-axis (0001) 4H-SiC substrates. The dielectric is AlN either as a single layer or in a stack with SiO_2, Al_2O_3 or Si_3N_4. AlN was grown in horizontal hot-wall MOCVD reactor at 1100°C [21,22]. Ammonia and $Al_2(CH_3)_6$ are used as a precursor for nitrogen and aluminium respectively. The details of the growth process are given in Ref. [22]. The samples investigated are summarized in Table 1. The additional layers of SiO_2, Al_2O_3 or Si_3N_4 were deposited by different methods. The SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) at 300°C using source gases of oxygen and silane. The Al_2O_3 was grown by atomic layer deposition (ALD) at 300°C via thermal decomposition of $Al_2(CH_3)_6$ in water ambient. In addition, Si_3N_4 layer was made by low pressure chemical vapor deposition (LPCVD) at 770^0C using source gases of ammonia and silane. The MOS capacitors were made by sputtering 0.5 µm thick aluminum as a gate metal, patterned by lithography and etching to form circular capacitors. Aluminum served as a backside contact as well. The reference samples with 32 nm or 37 nm thick SiO_2 grown in dry oxygen or in N_2O at 1240°C were analyzed. Another reference SiO_2 film was investigated which was made by intentional sodium contamination typically called sodium enhanced oxidation (SEO). In the SEO method, a 100 nm oxide was grown in O_2 ambient at 1240°C and densified in nitrogen medium at 1000°C for 5 h. This whole oxidation process was performed in alumina furnace tube with carrier boat made of sintered alumina. The alumina contains trace amounts of sodium which are responsible for increase in oxidation rate and for the reduction of interface traps [23].

Table 1. MOS devices used in this study.

No.	MOS structures	Thickness of dielectrics	Method of dielectric deposition
1	Al/AlN/SiC	10 nm	MOCVD at 1100°C
2	Al/AlN/SiC	30 nm	MOCVD at 1100°C
3	Al/SiO_2/AlN/SiC	40nm/10nm	PECVD at 300°C / MOCVD at 1100°C
4	Al/SiO_2/AlN/SiC	40nm/10nm	PECVD at 300°C then annealed at 900°C for 30 minutes / MOCVD at 1100°C
5	Al/Al_2O_3/AlN/SiC	40nm/10nm	ALD at 300°C / MOCVD at 1100°C
6	Al/Si_3N_4/AlN/SiC	40nm/10nm	LPCVD at 770°C / MOCVD at 1100°C
7	Al/SiO_2/Si_3N_4/AlN/SiC	10nm/40nm/10nm	PECVD at 300°C / LPCVD at 770°C / MOCVD at 1100°C

Room temperature CV measurements are performed on 300 µm circular Al pads of each sample using an Agilent E4980A LCR meter. The test frequencies were between 1 kHz and 1 MHz. The first estimate of the number density of interface states in MOS capacitors is done by investigating the frequency dispersion of the CV curves. Electron capture into interface states is most often a fast process while electron emission from interface traps is normally much slower and is a thermal process which depends on the difference E_c-E (where E is the energy level of the interface trap and E_c denotes the SiC conduction band edge). If an electron is captured and not emitted again this is detected as a shift of the CV curve to the high gate voltage. If the test frequency is high (1 MHz) then more traps will not emit their electrons and the curve is shifted to the high gate voltage as compared to the low frequency (1 kHz) curve [24]. The density of near-interface traps (NITs) is estimated by comparing GV data recorded at high gate voltage to theoretical data obtained from the distributed border traps model given by Yuan et al. [25]. IV measurements are made on 100 µm circular pads of sample 1 and sample 3 as well as on reference MOS samples using Keithley 617 electrometer. This IV technique is used to determine the dielectric breakdown strength and tunnel barrier height of these samples.

Some samples have electron traps that are located some distance into the dielectric and capture electrons from the semiconductor during accumulation bias stress which is detected as a shift in the CV curves. The trapped electrons do not return unless the temperature is raised and reverse electric field is applied for a long-time period. The number density of trapped electrons can be determined by using the expression $N_{it}=C_{ox} (V_{FB(f)}-V_{FB(s)})/qA$ where $V_{FB(f)}$ and $V_{FB(s)}$ are the flat band voltages of a fresh and of a stressed MOS sample respectively.

Results and discussion

Figure 1 shows room temperature CV spectra for AlN MOS samples 1 (10 nm AlN) and 3 (40 nm SiO_2/10 nm AlN). These MOS capacitors show a clear accumulation at positive voltages and depletion for negative voltages. The relative dielectric constant for AlN deduced from the accumulation capacitance is ~ 8.7. The flatband voltage is ~ 0.7 V which is close to the theoretical flatband voltage i.e. ~ 0.4 V which shows that initially the AlN layer contains insignificant amount of fixed charge. Here, CV data is shown for test frequencies between 1 kHz and 1 MHz and there is virtually no frequency dispersion in both samples which indicates that the single layer AlN and the SiO_2/AlN stack both contain low density of interface states. Leakage is observed in sample 1 above gate voltage of 3 V corresponding to an electric field of approximately 3 MV/cm across the AlN while the MOS capacitor with stacked dielectric shows no leakage up to 40 V gate bias (maximum bias for the CV meter). This shows that the addition of wide bandgap dielectric, i.e. SiO_2 on top of the AlN layer improves the breakdown voltage.

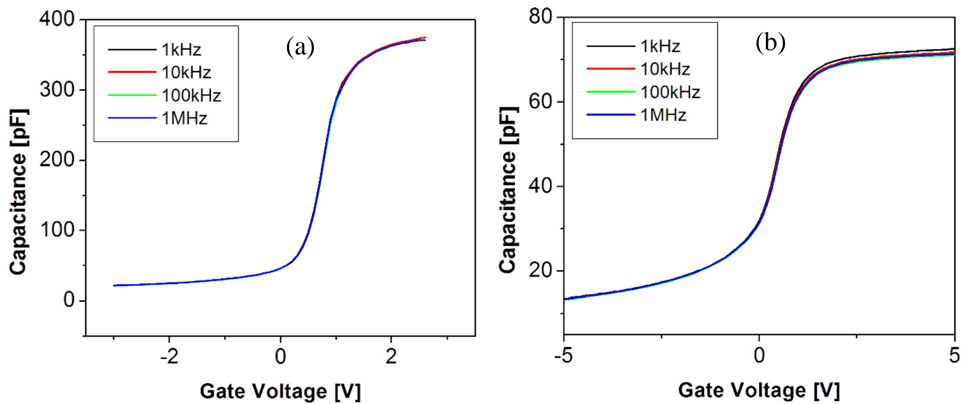

Figure 1. Room temperature CV curves for (a) sample 1 (AlN 10 nm) and (b) sample 3 (40 nm SiO_2/10 nm AlN) at four test signal frequencies between 1 kHz and 1 MHz.

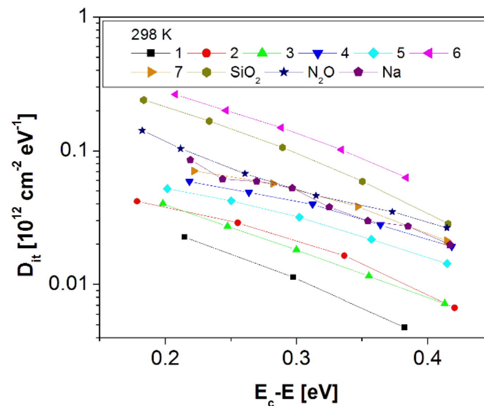

Figure 2. Comparison of the density of interface states (D_{it}) estimated from CV (at 298 K) as a function of energy for AlN MOS capacitors along with reference SiO_2 MOS capacitors.

Figure 2 shows the density of interface states as a function of energy near the SiC conduction band edge extracted from room temperatures CV for AlN samples as well as for three reference SiO_2 MOS capacitors. It is evident that sample 1, with a 10 nm thick layer AlN, has the lowest interface trap density of all the samples investigated including the SiO_2 reference samples. The detrimental interface states that exist within this energy range for all thermally grown oxides are virtually absent at the AlN/SiC interface. The thermal oxide made in the presence of Na (labeled Na in Figure 2) has very low density of interface states and the field effect mobility in MOSFETs made with this oxide is ~ 150 cm^2/Vs which is among the highest reported [23]. This suggests that high mobility could be achieved in AlN based MOSFETs.

The thickness of the AlN affects the AlN/SiC interface quality. Sample 2 with a 30 nm thick AlN layer has higher density of interface states than the 10 nm thick sample but nevertheless much lower than in the thermal oxide samples. This is not surprising since the density of misfit dislocations increases with increasing AlN thickness and above approximately 30 nm they can cause a deterioration of the insulating properties of AlN films in MOS devices [26]. It is also clear that dielectric stack does in general have higher interface state densities than a single AlN layer. So, the addition of different dielectric layers on the top of AlN affects the AlN/SiC interface quality of the AlN stack samples, the Si_3N_4/AlN stack (sample 6) has the highest interface trap density. This can be a result of the high temperature (770^{0}C) growth of Si_3N_4 on the top of AlN that might have affected the AlN/SiC interface. The SiO_2/AlN stack (sample 3) has the best result for a stack in terms of density of interface states and is comparable to a 30 nm single AlN layer (sample 2).

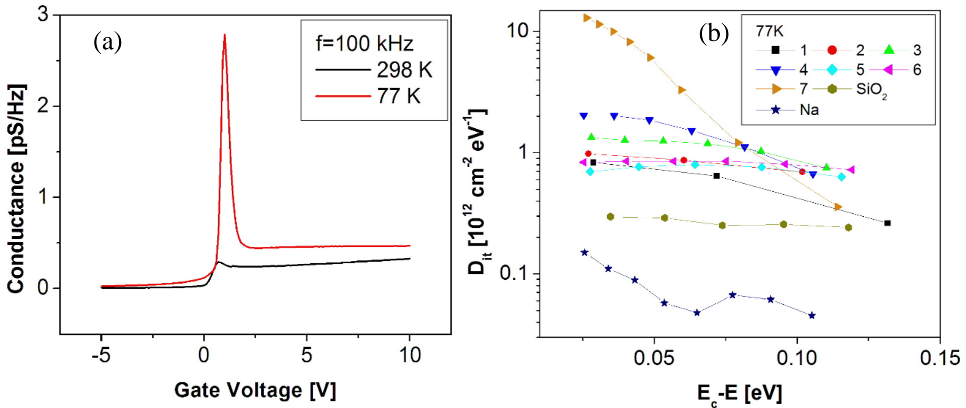

Figure 3. a) GV curve (100 kHz) for sample 3 at 298 K and 77 K. b) Interface state density as a function of energy for AlN and reference SiO_2 MOS capacitors at a temperature of 77 K.

Figure 3a shows 100 kHz GV curves for sample 3 performed at 298 K and 77 K. In the GV profile, the conductance peak occurs near flatband conditions and is due to response from interface traps near the fermi level [24]. The conductance peak height gives a rough estimate of the presence of interface traps near the fermi level. There is a striking difference in the height of conductance peak for 298 K and 77 K. This indicates that AlN sample has very fast shallow traps that are only possible to detect at low temperature.

Therefore, the shallow interface traps density was extracted from CV data at 77 K for AlN samples and reference SiO_2 MOS capacitors and the result is shown in figure 3b. At 77 K, a high density of shallow interface traps is seen in all AlN MOS samples. The AlN samples even have higher shallow trap density than the reference SiO_2 samples. The interface trap density results of the AlN samples expressed in figure 2 and 3b (for 298 K and 77 K respectively) show good agreement with the conductance peak height observed in figure 3a. The impact of these shallow traps on channel mobility in MOSFETs is not known but they are very fast at room temperature compared to the detrimental interface traps at the SiO_2/SiC interface.

The number density of NITs that are located at some distance (1-2 nm) inside the dielectric in a MOS device can be determined by using a distributed border traps model presented by Yuan et al. [25]. By this model, we calculate the admittance profile of the MOS capacitor with border traps or in other words near-interface traps (NITs) and compare them with experimental CV and GV results recorded in the accumulation region. In strong accumulation, the series resistance (R_s) can play a significant role especially in the conductance curve. Therefore, it is necessary to extract the R_s value and include its influence on the calculated admittance profile. As proposed by Yu et al., R_s can be extracted by plotting the measured data, $G_m/\omega C_m^2$, against frequency, ω. [27]. We have used this model to estimate the NITs based on the conductance data in accumulation, taking also into account the effect of R_s. The experimental conductance data at 77 and 298 K is used to estimate the NITs. In the simulations presented here the energy level of the NITs is assumed to be 0.1 eV above the SiC conduction band edges but the exact energy level position has a minor impact on the overall result. An example of experimental conductance data and the results of such a fitting procedure is shown in figure 4.

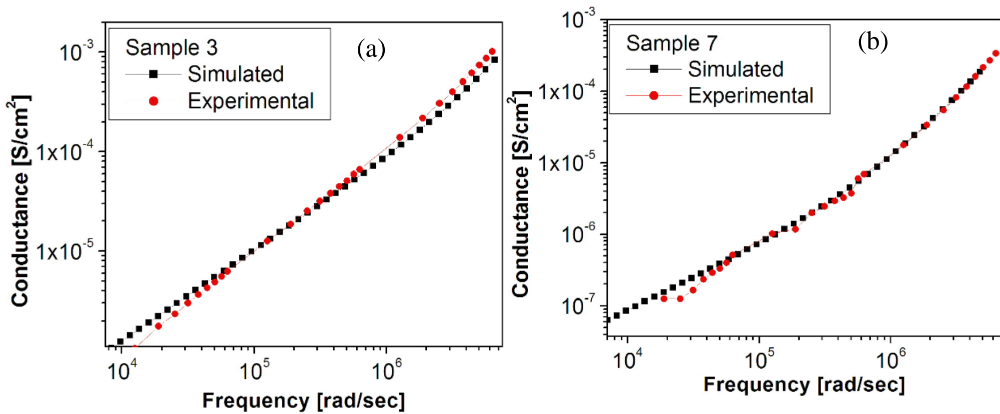

Figure 4**:** Simulated and low temperature (77 K) experimental conductance data at 10 V gate voltage for (a) sample 3 and (b) sample 7.

Figure 4 shows the simulated and low temperature (77 K) experimental conductance data of AlN MOS samples 3 and 7 at a gate voltage of 10 V. The key fitting parameters are NITs and R_s [28]. The extracted value of active NITs at 77 K and 298 K are given in table 2 below. The typical value of the extracted R_s is in the range 1-3x10^{-3} (Ωcm^2). In the case of AlN single layers (samples 1 and 2) gate leakage is observed in accumulation at rather low gate voltages (at an electric field of ~ 3 MV/cm) which excludes the usage of this

accumulation conduction method. Table 2 shows that the volume density of NITs in the thermal oxide reference samples is reduced with lowering temperature. It is a typical behavior because electron traffic between NITs and conduction band of SiC is to a certain extent thermally activated [28,29]. Such a large reduction in the volume density of NITs with reducing temperature is not seen in AlN samples except in sample 6. Samples 4 has the lowest volume density of NITs compared to the other investigated AlN MOS samples at both temperatures (77 K and 298 K). This indicates that the high temperature (900°C) annealing of SiO_2 of sample 4 and the high temperature growth of Si_3N_4 dielectric of sample 6 do have a negative impact on the density of interface traps (as shown in figure 2) but this high temperature seems to play a role in reducing the density of NITs.

Table 2: Volume density of NITs in differently prepared AlN MOS devices and in thermally grown reference SiO_2 samples, extracted by comparing simulated and experimental conductance data at 77 K and 298K.

Sample	NITs 298K (cm^{-3})	NITs 77K (cm^{-3})
3	~ 2.5×10^{18}	~ 3.3×10^{18}
4	~ 2×10^{17}	~ 1×10^{17}
5	~ 3×10^{18}	~ 1.3×10^{18}
6	~ 4×10^{18}	~ 3×10^{17}
7	~ 2×10^{18}	~ 1.5×10^{18}
SiO_2	~ 2×10^{19}	~ 2.5×10^{18}
N_2O	~ 5×10^{18}	~ 6×10^{17}
Na	~ 3×10^{17}	~ 6×10^{16}

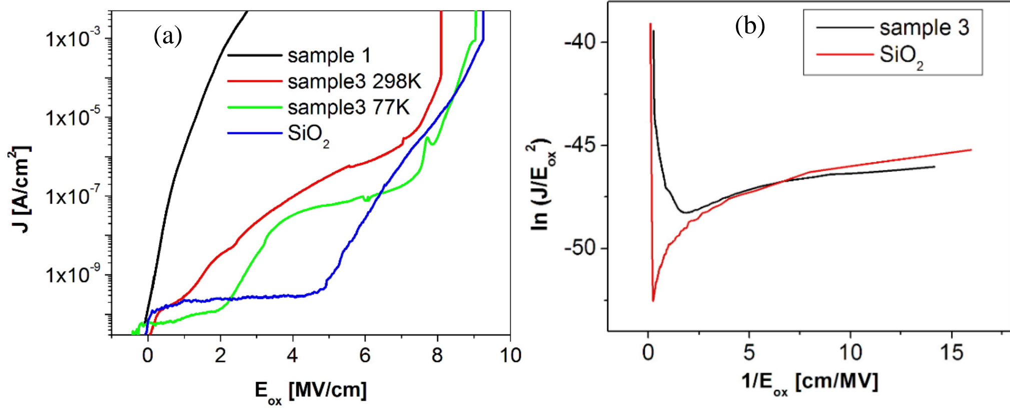

Figure 5. (a) Comparison of leakage current density versus electric field (J-E) of sample 1 and 3 and of dry thermal SiO_2. J-E profile of sample 3 is shown for 298 K and 77 K. (b) The F-N plot for sample 3 and for dry SiO_2 at room temperature.

Figure 5(a) compares the dielectric breakdown field of sample 1 and 3 along with thermally grown dry SiO_2 reference sample based on current density measurement as a function of the electric field (J-E) across the gate dielectric. IV measurement of sample 3 was done at 298 K and 77 K to see the effect of temperature on the dielectric breakdown. A slight decrease in the current leakage is observed when the temperature is lowered to 77 K. A breakdown field of approximately 3 MV/cm is observed in sample 1 and the same value was observed in sample 2 (not shown here). A breakdown field of 3 MV/cm is also reported in literature for a single layer AlN [18,26,30]. This breakdown field is very low compared to the breakdown field of reference thermal SiO_2 MOS capacitors which is ~ 9 MV/cm. For sample 3 composed of AlN and SiO_2 (room temperature red curve in figure 5a), the effective electric field, $E_{eff} = \frac{V_G - V_{FB}}{t_{ox,total}}$ if we consider the dual dielectric as a single dielectric [31], is ~ 8 MV/cm. The electric field, however, across the required dielectric layer, AlN, in sample 3 is determined by using the expression $E_{AlN} = \frac{V_G - V_{FB}}{t_{AlN}} \times \frac{C_{ox,SiO2}}{C_{ox,SiO2} + C_{ox,AlN}}$, taking into account the mismatch in dielectric constants [31]. This expression gives the breakdown field value of ~ 4 MV/cm across the AlN dielectric in the stack. This shows that an addition of the wide bandgap dielectric, SiO_2, on the top of AlN layer slightly improves the breakdown field. The actual benefit of the AlN stack MOS capacitor is that it can tolerate higher gate voltages compared to a single layer AlN.

Figure 5a shows that the current leakage behavior across the dielectric is different in the single layer AlN and the stacked AlN MOS sample. F-N tunneling behavior is seen in the SiO_2/AlN stack (sample 3) and the reference sample while an abrupt leakage is observed in the single layer AlN (sample 1). This suggests that the SiO_2 layer on top of the AlN layer blocks the current leakage across the AlN layer. The J-E data of sample 3 (red curve) and the reference sample (blue curve) was analyzed to determine the tunneling barrier heights assuming F-N tunneling mechanism. The classical expression for F-N tunneling is

$$J = AE_{ox}^2 \exp\left(\frac{-B}{E_{ox}}\right)$$

$$A = \frac{q^3 m_{SiC}}{8\pi h m_{ox} \phi_b}, \quad B = \frac{8\pi\sqrt{2m_{0x}}\,\phi_b^{\frac{3}{2}}}{3hq}$$

Here, q is the electron charge, m_{sic} and m_{ox} are the effective electron masses in the SiC and the oxide respectively, h is the Planck constant, E_{ox} is the electric field in the oxide and ϕ_b is the effective barrier height in eV measured from the SiC conduction band edge to the oxide conduction band edge. The effective barrier height is mostly determined by parameter B by taking the slope of the straight line appearing in a F-N plot at high electric fields. Such a plot is shown in figure 5(b). AlN/SiC and SiO_2/SiC barrier heights of 1.60 eV or 2.50 eV are obtained respectively by assuming the value of m_{ox} of AlN and SiO_2 to be 0.4m_o and 0.42m_o respectively. The barrier height of SiO_2/SiC interface was found to be 2.43 eV at room temperature using F-N tunneling mechanism in ref. [32] and this value is reasonably close to the barrier height extracted from our IV analysis. The AlN/SiC barrier height determined by XPS is 1.7 eV in Ref. [17] and this value is also close to the barrier height extracted in our case by IV analysis.

A sensitivity to electron injection is observed in the AlN samples. This is detected as a flatband shift in subsequent CV curves when the sample is repeatedly biased into accumulation. Dislocations are reported to appear in AlN films thicker than 6 nm [26]. In our case the thickness is 10 nm so this flatband shift can be a result of trapping of electrons in dislocations or at some intrinsic defects within the AlN. Similar electron injection is also observed in the dielectric stacks containing AlN. The trapped electrons are released back to the SiC if depletion bias is applied to the MOS capacitors at elevated temperatures. However, this is not the case for the samples that have Al_2O_3/AlN and Si_3N_4/AlN stacks where the flatband shift remains stable. The conduction band offsets between the stacked dielectrics in this case are very small and it is possible that the electrons are injected into the Al_2O_3 or Si_3N_4 during the accumulation bias stress.

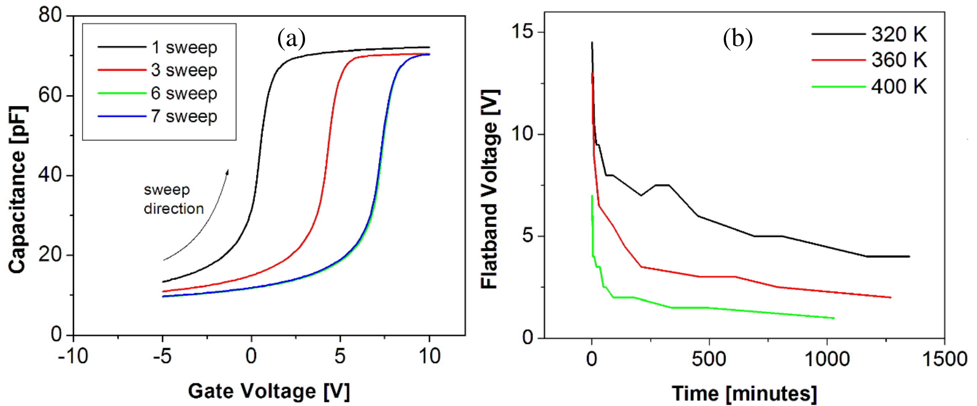

Figure 6. (a) Subsequent 100 kHz CV sweeps for sample 3 at room temperature. Electrons are injected into the AlN layer during accumulation bias which is detected as positive flatband voltage shift. (b) Electron emission from traps within the AlN observed as a negative shift in the flatband voltage. CV sweeps are made subsequently at different time intervals at a given fixed temperature from depletion to accumulation.

Figure 6a shows electron injection into the AlN layer in sample 3. The shift of the CV curve saturates after several gate voltage sweeps from depletion to accumulation (-5 V to 10 V respectively). However, the magnitude of the shift depends on the maximum applied accumulation voltage (which in this case is 10 V). It is evident that the shift is because of the electron capture within the AlN under accumulation bias and the electron do not return when the sample is biased to depletion. Charge trapping in AlN is commonly reported in literature [8,16]. In our case, the flatband shift after stressing is here about 7 V which corresponds to an effective negative trapped charge of ~ 4×10^{12} cm^{-2}. These trapped electrons can be released back to the SiC by applying depletion bias (-5 V gate voltage) at elevated temperatures to the MOS capacitor. An example of such experiment is shown in figure 6(b). The traps within the AlN are first intentionally filled with electrons at room temperature by applying accumulation bias of 20 V for 10 minutes. Thereafter, subsequent CV sweeps are made from depletion to weak accumulation (< 20 V) at different time intervals and the flatband voltage is monitored. This experiment is performed at three different temperatures of 320 K, 360 K and 400 K. Applying high temperature under depletion enhances the rate of electron emission. This experiment demonstrates that the net negative charge observed in these AlN layers is not a permanently fixed charge but rather electrons trapped within the dielectric which can be released to the SiC using depletion bias and by raising the temperature of sample.

In summary, the AlN MOS samples show some very interesting results. Based on room temperature CV analysis, the AlN/SiC interface contains very low density of interface states compared to state of the art thermal oxides. The density of active near-interface traps at room temperature based on conductance analysis is also lower than in all refence thermal oxides except the SEO oxide. However, it is evident that the AlN/SiC interface has significant amount of fast interface states located very near the SiC conduction band edge. These interface state are detected at 77 K in capacitance and conductance analysis and could have an impact on electron channel mobility in AlN based SiC MOSFETs. Overall the results are very promising in terms of interface state densities but the main obstacle here is severe electron injection into the AlN under accumulation bias. This is related to the low barrier height (1.6 eV) between the AlN and the SiC. The physical origin of the electron traps within the AlN is unknown but if they are related to structural defects their density could be reduced by growing thinner layers of AlN (2-3 nm) and then depositing SiO_2 on top of the AlN to complete the dielectric stack.

Conclusions

CV analysis at room temperature reveals an order of magnitude lower density of interface traps at the AlN/SiC interface than at nitrided SiO_2/SiC interfaces. It is evident that the interface traps that are held responsible for electron channel mobility reduction in 4H-SiC MOSFETs are practically absent at the AlN/SiC interface in this study. The AlN/SiC structures do have a large density of fast interface traps located very near the SiC conduction band edge that are revealed by CV analysis at 77 K and could have some impact on the electron channel mobility. Electron trapping within the AlN is significant when the MOS capacitors are biased into accumulation resulting in a large flatband voltage shift towards higher gate voltage. This process is reversible and the electrons are fully released from the AlN layer if depletion bias is applied at elevated temperatures. This is connected to the relatively low breakdown field (3-4 MV/cm) of the AlN layers. It is possible to improve the breakdown field slightly by depositing a SiO_2 layer on top of the

AlN. For future studies, we propose growing a few nm thin AlN layer followed by a thick layer of deposited SiO_2 in an attempt to decrease the electron trapping within the AlN layer. More work is needed on such dielectric stacks to reveal if they can be an alternative to SiO_2 as a gate dielectric in 4H-SiC MOS devices.

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Paper D

Electrical characterization of amorphous Al_2O_3 dielectric films on n-type 4H-SiC

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manuscript submitted for publication.

Electrical characterization of amorphous Al_2O_3 dielectric films on n-type 4H-SiC

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Abstract. We report on the electrical properties of Al_2O_3 films grown on 4H-SiC by successive thermal oxidation of thin Al layers at low temperatures (200°C - 300°C). MOS capacitors made using these films contain lower density of interface traps, are more immune to electron injection and exhibit higher breakdown field (5MV/cm) than Al_2O_3 films grown by atomic layer deposition (ALD) or rapid thermal processing (RTP). Furthermore, the interface state density is significantly lower than in MOS capacitors with nitrided thermal silicon dioxide, grown in N_2O, serving as the gate dielectric. Deposition of an additional SiO_2 film on the top of the Al_2O_3 layer increases the breakdown voltage of the MOS capacitors while maintaining low density of interface traps. We examine the origin of negative charges frequently encountered in Al_2O_3 films grown on SiC and find that these charges consist of trapped electrons which can be released from the Al_2O_3 layer by depletion bias stress and ultraviolet light exposure. This electron trapping needs to be reduced if Al_2O_3 is to be used as a gate dielectric in SiC MOS technology.

1. Introduction

4H-SiC metal-oxide semiconductor field-effect transistors (MOSFETs) are promising devices for power electronics. Such transistors are now commercially available for blocking voltages above 900 V [1,2]. These devices provide higher switching speeds and lower switching losses than Si MOSFETs. However, SiC MOSFETs cannot compete with Si technology for lower blocking voltages because of poor electron channel mobility which limits the device on-resistance. A key problem is the high density of so called near-interface traps (NITs) detected at the SiO_2/4H-SiC interface with energy levels near the SiC conduction band edge that limit the electron channel mobility [3-6]. Currently thermal oxides grown or annealed in NO or N_2O are the mainstream dielectrics but more reduction in NITs is needed [7]. Other large bandgap dielectrics such as AlN, Al_2O_3 and HfO_2 have also been investigated [8-14]. One of the alternatives is aluminum oxide (Al_2O_3) with bandgap of ~ 7.0 eV [8,11,15]. Recently, an amorphous Al_2O_3 has been used as a gate dielectric in graphene field effect transistors with some success [16,17]. Those Al_2O_3 films are grown by atomic layer deposition (ALD) at 300°C or thermal evaporation of metallic Al followed by low temperature oxidation to form Al_2O_3 [16,17]. As grown Al_2O_3 deposited on 4H-SiC by ALD typically contains a large number of negative charges which are reduced after annealing in Ar at 1000°C but the Al_2O_3/SiC interface contains a high density of interface traps after such treatment [9,10]. More recently, studies on pre-deposition surface cleaning and post deposition annealing at different temperature in N_2O

ambient are been performed on ALD grown Al_2O_3. A high density of negative charge is observed in such samples and after post deposition annealing at 1000°C, an interfacial SiO_x ($0 < x < 2$) layer grows containing a high density of interface traps [18]. There is a report on a very high peak field effect mobility of 300 cm^2/Vs in SiC MOSFETs using Al_2O_3 made by metal-organic chemical vapor deposition (MOCVD) with a thin SiO_2 interfacial layer to the SiC [13]. But, the mobility drops very rapidly with gate voltage and is less than 50 cm^2/Vs at moderate gate voltages. Recently, a MOSFET with ALD grown Al_2O_3, that was post-annealed in hydrogen at 400°C, was reported with a field effect mobility of 57 cm^2/Vs. Even though these results are promising the Al_2O_3 layers were sensitive to electron injection resulting in large threshold voltage shifts of the MOSFETs [19]. In previous studies, a careful attention has not been paid to the origin of negative charges within the Al_2O_3 which normally are assumed to be a fixed oxide charge. In this work, we studied the interface quality of differently prepared Al_2O_3/4H-SiC interfaces, the breakdown properties of the Al_2O_3 dielectrics as well as the origin of negative charges within the Al_2O_3. Recently, we reported a very low density of NITs in Al_2O_3 layers formed on 4H-SiC by thermal oxidation of Al [20]. In this work, we investigate these layers in more detail and compare them with Al_2O_3 layers grown by ALD or RTP. We find that is it possible to grow Al_2O_3 films with negligible negative charge and very low density of interface states at the Al_2O_3/4H-SiC interface.

2. Experimental methods

The SiC samples used in this study consist of 10 µm thick n-type epitaxial layers, with a net doping concentration of ~ $1x10^{16}$ cm^{-3}, grown on 4 degrees off-axis (0001) 4H-SiC substrates. The Al_2O_3 layers are grown on the 4H-SiC substrates by different deposition methods. Prior to deposition all samples were cleaned with HF in order to remove the native oxide. In one of the deposition methods, a 1-2 nm thick Al metal layer is deposited by electron beam evaporation of Al in a vacuum chamber at a rate of 0.5 Å/s and then immediately the sample is baked on a hot plate at a temperature of 200°C for 5 minutes to form Al_2O_3 layer [16,17,21]. This process of deposition and subsequent oxidation is repeated twelve times to get target thickness of ~ 15 nm with an overall time span of about 4 hours. We refer to this method as hot plate Al_2O_3. A hot plate Al_2O_3 sample was grown at 300°C as well and we found no difference in the electrical properties of these samples. A stack of SiO_2/Al_2O_3 was made by growing a thick layer of 40 nm of SiO_2 on the top of the hot plate Al_2O_3 by plasma enhanced chemical vapor deposition (PECVD) at 300°C using source gases of oxygen and silane. An Al_2O_3 layer of 15 nm thickness was also grown by ALD at 300°C via thermal decomposition of $Al_2(CH_3)_6$ in water ambient. In addition, Al_2O_3 films were made by using rapid thermal processing (RTP). The RTP Al_2O_3 samples were prepared by oxidation of pure Al metal and subsequent rapid thermal annealing in oxygen ambient. 6 nm of Al was deposited onto four separates SiC samples and subsequently oxidized at 500°C, 600°C, 700°C, and 1000°C for 30 min, 30 min, 15 min, and 5 min respectively. The oxidation cycle was repeated twice to achieve a target film thickness of 15 nm after oxidation. Apart from the sample made at 1000°C, the resulting oxides were too leaky for CV characterization. The oxide thickness of all samples was estimated using X-ray reflectivity (XRR) and the crystallinity was investigated with X-ray diffraction (XRD) apart from the RTP grown samples. Our Al_2O_3 films in this study are amorphous with no crystallization observed by XRD. The chemical composition of the films has not been verified here experimentally but previous studies using similar growth methods reveal the formation of amorphous Al_2O_3 [22]. Reference samples with 20 nm

thick thermal SiO_2 grown in dry oxygen (at 1150°C for 90 min) as well as 37 nm thick thermal SiO_2 grown in N_2O (1240°C for 90 min) were also analyzed. The Al_2O_3 samples are summarized in Table 1 below.

Table 1. Summary of Al_2O_3 MOS samples used in this study.

No.	MOS structures	Thickness of oxide	Method of oxide deposition
1	$Al/Al_2O_3/SiC$	~ 15 nm	Hot plate at 200°C
2	$Al/SiO_2/Al_2O_3/SiC$	~ 40 nm /15 nm	SiO_2 by PECVD at 300°C / Al_2O_3 by hot plate at 200°C
3	$Al/ Al_2O_3/SiC$	~ 15 nm	ALD at 300°C
4	$Al/ Al_2O_3/SiC$	~ 15 nm	RTP at 1000°C

Circular n-type MOS capacitors were made using Al as a gate metal. The backside contact was formed by thick Ni (100nm) metallization. The capacitance- and current-voltage measurements (CV and IV) are performed on circular MOS pads, with diameter of 300 µm, using Agilent E4980A LCR meter and Keithley 617 electrometer respectively. To estimate the interface quality of Al_2O_3/SiC interface, conventional CV measurements are performed at room temperature and at different frequencies ranging from 1 kHz to 1 MHz, while to examine the negative charges within the Al_2O_3, room temperature CV measurements are made using UV light illumination. IV measurements are used to examine the leakage current characteristics, the critical breakdown field and the tunneling barrier height of the dielectric Al_2O_3.

3. Results and discussion

Figure 1 shows CV spectra of aluminum oxide MOS capacitors measured at room temperature and at 1 kHz and 1 MHz frequencies. The gate bias is swept from depletion (negative bias) to accumulation (positive bias) and the capacitance signal for both frequencies is recorded simultaneously at each gate bias point. Figure 1(a) shows the CV curves for a hot plate Al_2O_3 sample. The dielectric constant deduced from the capacitance in accumulation (5 V) is about 6.5. A first estimate of the interface trap density is extracted from frequency dispersion of CV curves [23]. In this case, such dispersion is hardly visible indicating a rather low interface state density. Figure 1(b) shows the CV spectra of the SiO_2/hot plate Al_2O_3 dielectric stack. Small frequency dispersion is observed indicating some increase in the interface state density. Figure 1(c) shows the CV spectra for ALD grown Al_2O_3. Two noticeable features are observed in the low frequency (1 kHz) CV curve. A “hump” at ~ 0 V suggests the presence of specific rather deep interface traps that are not able to follow the 1 MHz test signal. Secondly the capacitance in accumulation is higher than the 1MHz curve and this is due to current leakage through the oxide which distorts the 1 kHz measurement. Figure 1(d) shows the CV spectra for the RTP grown Al_2O_3. A very large frequency dispersion reveals high density of interface states.

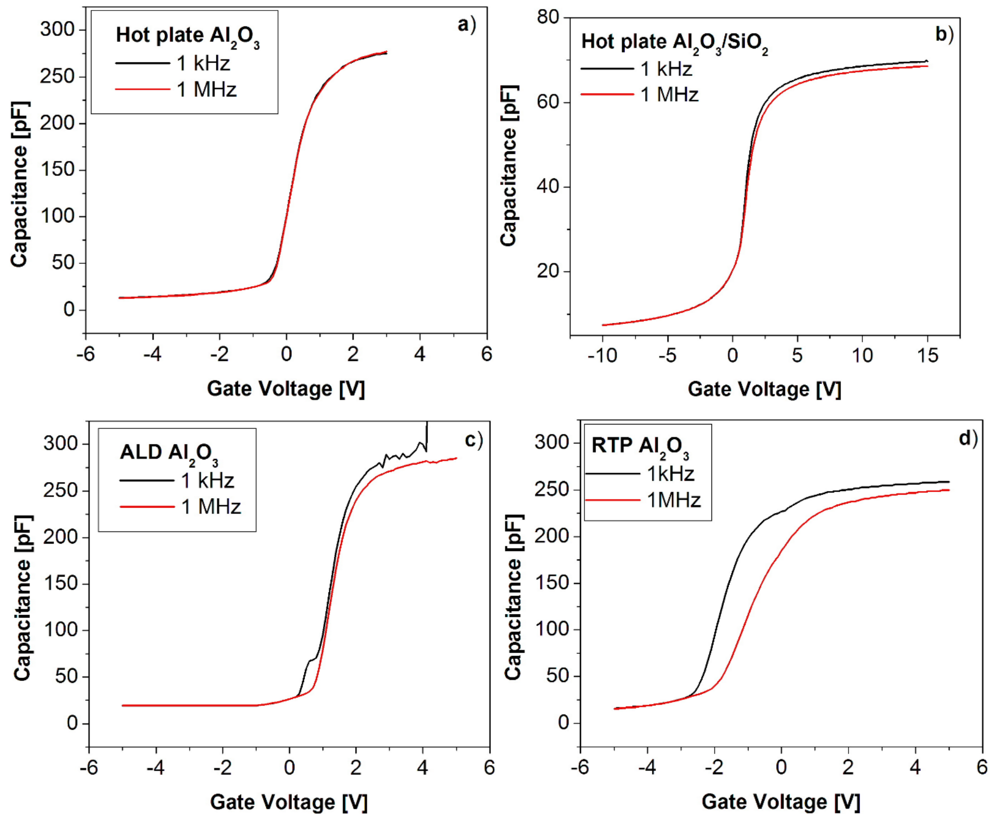

Figure 1 CV curves at room temperature of: (a) a hot-plate Al_2O_3 MOS capacitor (b) a dielectric stack of SiO_2/hot plate Al_2O_3 (c) ALD grown Al_2O_3 and (d) RTP grown Al_2O_3.

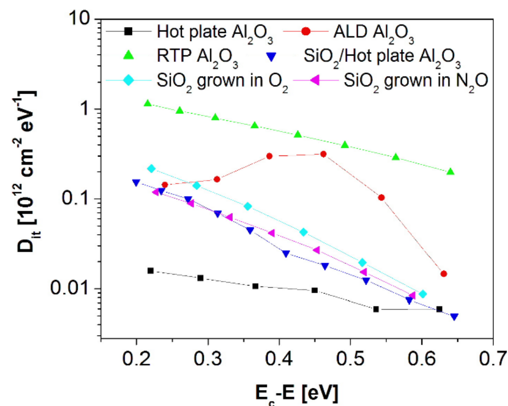

Figure 2 Density of interface states (D_{it}) as a function of energy from the SiC conduction band edge, extracted from CV analysis at room temperatures for the sole and stack Al_2O_3 dielectric samples grown by different methods and samples with thermal SiO_2 grown in O_2 or N_2O ambient.

Figure 2 compares the interface state density in the different Al_2O_3 samples extracted from frequency dispersion of room temperature CV data (between 1kHz and 1 MHz) together with data from reference samples with thermal SiO_2 made in dry oxygen or N_2O ambient. It is evident in figure 2 that the hot plate Al_2O_3 sample contains the lowest density of interface traps. The interface state density in the Al_2O_3 stack sample is comparable with nitrided reference SiO_2 sample but is lower than in reference SiO_2 grown in O_2. The ALD grown Al_2O_3 shows a peak in the interface state density at energies between 0.35-0.55 eV from the SiC conduction band edge. RTP grown Al_2O_3 has relatively high density of interface traps.

The MOS capacitors were investigated by IV as well at room temperature. Leakage current density vs electric field (J-E) curves for several different samples are shown in figure 3(a). The sole hot plate Al_2O_3 has breakdown field (~ 5 MV/cm) which is higher than the ALD and RTP grown Al_2O_3 films. This value of the breakdown field is about half the breakdown field achieved in the reference SiO_2/SiC MOS capacitor (light blue curve in figure 3(a)). Reported breakdown field of Al_2O_3 on SiC varies in literature and the highest value, to our knowledge, is approximately 8 MV/cm in amorphous ALD grown films [11]. However, in that study the leakage current density prior to breakdown was of the order of 10^{-3} A/cm^2 which is few orders of magnitudes higher than in the hot-plate grown Al_2O_3. In case of the SiO_2/Al_2O_3 stack (dark blue curve in figure 3a), the effective breakdown field, $E_{eff} = \frac{V_G - V_{FB}}{t_{ox,total}}$ treating the dual dielectric as a single dielectric, is ~ 8 MV/cm. Here V_G, V_{FB} and $t_{ox,total}$ are the gate voltage, flatband voltage and the thickness of the dielectric stack respectively. A steep increase in the current is observed around 5 MV/cm but before that the leakage current value is relative low around 10^{-8} A/cm. The breakdown field across the Al_2O_3 dielectric can be determined by considering the difference of the dielectric constants in the stack using the expression $E_{Al2O3} = \frac{V_G - V_{FB}}{t_{Al2O3}} \times \frac{C_{ox,SiO2}}{C_{ox,SiO2} + C_{ox,Al2O3}}$ [24]. Here t_{Al2O3} denotes the thickness of Al_2O_3. $C_{ox,SiO2}$ and $C_{ox,Al2O3}$ are the calculated capacitances of SiO_2 and Al_2O_3 respectively by taking into account the corresponding dielectric constant and thickness of the dielectric. This expression gives the breakdown field value of ~ 5.5 MV/cm across the Al_2O_3 dielectric in the stack. This indicates that the addition of SiO_2 layer on top of the hot plate Al_2O_3 has not much impact on the breakdown field of Al_2O_3 but the benefit of stack dielectric MOS capacitor is that it can operate at higher gate voltages.

Significant Fowler-Nordheim (F-N) tunneling is seen in the J-E profile of the sole hot plate Al_2O_3 and reference dry SiO_2 MOS sample. Therefore, the J-E response of these MOS sample was analyzed further using F-N tunneling mechanism to determine the tunneling barrier height. F-N tunneling current density across MOS devices at high field is described by [25]

$$J = AE^2 \exp\left(\frac{-B}{E}\right) \qquad (1)$$

Where, $A = \frac{q^3 m}{8\pi h m_{ox} \phi_b}$ and $B = \frac{8\pi\sqrt{2m_{ox}}\,\phi_b^{\frac{3}{2}}}{3hq}$. The parameters A and B depend on the tunneling barrier height ϕ_b and the effective mass of the tunneling electron m_{ox} in the oxide. A and B, can be derived from the experimental IV characteristics plotted as *ln* (J/E^2) *vs.* $1/E$, a so-called F-N plot. The slope of the straight line at high electric fields gives B while

A is determined from the intercept. Since *B* is the exponent in equation (1) for F-N tunneling current density, it is the prominent parameter in determining the current flow in the gate oxide [25].

Figure 3(b) shows F-N plot for a hot plate grown Al_2O_3 and for a reference dry SiO_2. The value of parameter *B* is 38 MV/cm and 175 MV/cm for Al_2O_3 grown by hot plate and for reference dry SiO_2 respectively. The effective barrier height for the hot plate grown Al_2O_3/4H-SiC interface extracted from this analysis is 1.15 eV by taking effective electron mass in Al_2O_3 to be $0.2m_o$ where m_o is the free electron mass [11]. A SiO_2/4H-SiC barrier height of 2.50 eV is obtained by assuming m_{ox} in SiO_2 is $0.42m_o$ [26]. This barrier height of the reference SiO_2/4H-SiC MOS sample is reasonably close to the previously reported values for dry SiO_2 determined by F-N tunneling mechanism [26]. The highest barrier height in literature for amorphous ALD grown Al_2O_3/4H-SiC, determined by F-N tunneling mechanism, is 1.58 eV as compared to 1.15 eV in our hot-plate [11]. This indicates that the hot plate Al_2O_3/4H-SiC interface has some defect states that limit the oxide breakdown field.

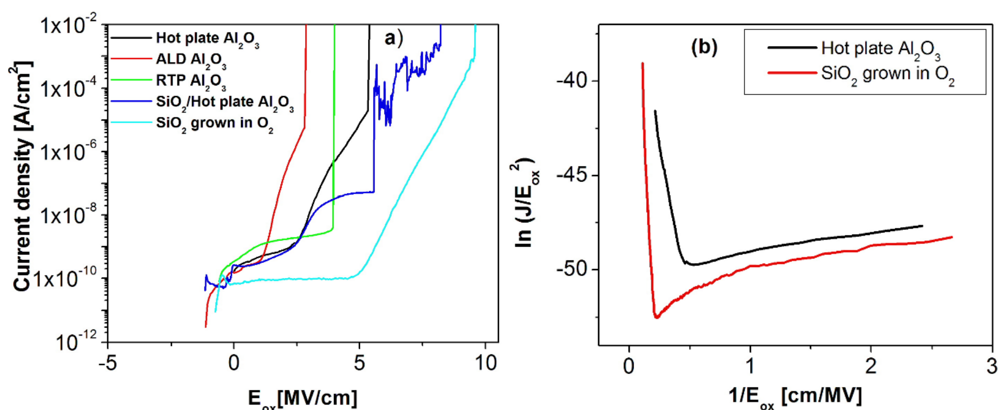

Figure 3 (a) Comparison of leakage current density vs electric field across the oxide (J-E) of differently prepared Al_2O_3 along with a reference sample with thermal SiO_2 grown in O_2, (b) A Fowler-Nordheim plot for hot plate grown Al_2O_3 and for dry SiO_2.

The Al_2O_3 samples are all found to be sensitive to electron injection except the RTP grown Al_2O_3. RTP grown Al_2O_3 may have a thin interface layer of SiO_2 that forms during the high temperature treatment as reported in literature [9,10,18]. The electron injection is observed by a shift of the CV curve after applying accumulation bias. Figure 4 shows such examples for hot plate and ALD grown Al_2O_3 samples. Repeated sweeps from depletion to accumulation result in a positive flatband voltage shift which saturates after several sweeps. This saturation has not been observed in the SiO_2/hot plate Al_2O_3 stack. The magnitude of the shift depends on the maximum accumulation voltage (in this case 5 V) and is larger in the ALD grown Al_2O_3. It is evident that electrons are trapped in the dielectric under accumulation bias and do not return to the SiC when the samples are biased in depletion. The electron charge trapped in the hot plate Al_2O_3 is approximately 3.4×10^{12} cm^{-2} and ~ 5.0×10^{12} cm^{-2} in the ALD Al_2O_3. This is significantly lower than previously reported in as grown ALD films where the densities are typically in the $1\text{x}10^{13}$ cm^{-2} range or higher [9-11].

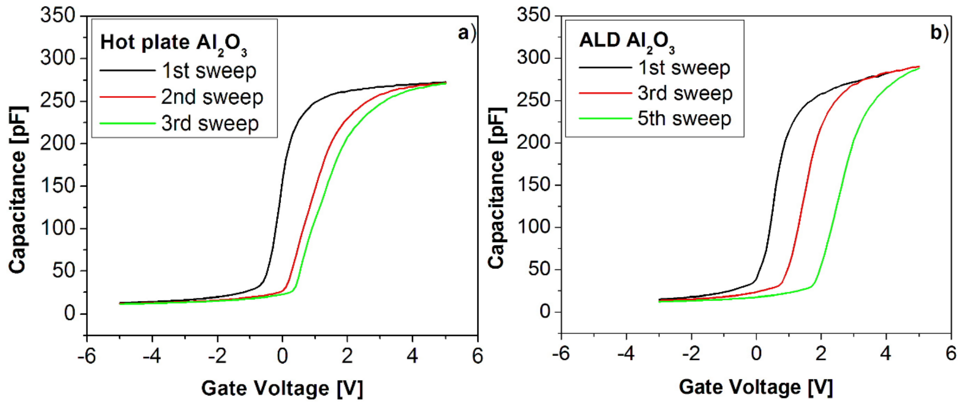

Figure 4 (a) CV spectra of a hot plate Al_2O_3 sample upon repeated gate voltage sweeps from depletion to accumulation, (b) the same experiment for ALD grown Al_2O_3. The shifts of the CV curves are due to trapping of electrons within the Al_2O_3 under strong accumulation bias which saturates after several sweeps.

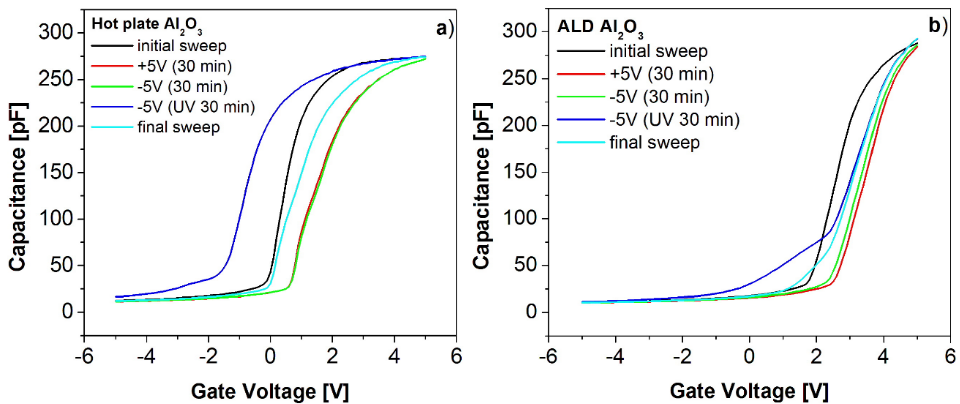

Figure 5 CV characteristics (100 kHz) at 300 K of (a) hot plate- and (b) ALD- grown Al_2O_3 samples before and after applying positive or negative bias stress to them. The black curves denote the first reference curves made after obtaining stable flatband voltage at 300 K (see figure 4). The light blue curves are the final curves recorded at the end of the experiment. For details see main text.

We examined the existence of electron capture and emission from traps within the aluminum oxide by using bias stress and UV illumination. The UV light was provided with a fluorescent lamp with mercury lines providing carrier generation across the 4H-SiC bandgap. Figure 5 shows the results of such an experiment for different Al_2O_3 samples at room temperature. The first reference CV (black curve) sweep is from depletion to accumulation on MOS pads after a stable flatband voltage is reached (as in figure 4) The MOS capacitor is then kept in accumulation (+5 V) for 30 minutes and then the bias is swept from depletion (-5 V) to accumulation (+5V) and the CV (red curve) is recorded.

Electrons are injected into the oxide during the accumulation bias stress and electron trapping is detected as a positive flatband shift.

Next, a depletion bias of -5 V is applied for 30 min to examine if electrons are released from oxide traps under such conditions. The CV (green curves) are recorded directly thereafter and are almost identical to the curves recorded after accumulation bias stress CV (red curves) showing that there is insignificant release of electrons from oxide traps. Next, ultraviolet (UV) light is applied to the sample under depletion bias (-5 V) for 30 min. A negative flatband voltage shift of about 2 V is observed in the hot plate Al_2O_3 sample in the CV sweep following the UV light illumination (dark blue curve). It is evident that electrons trapped in the Al_2O_3 are released during the UV exposure. The number density of released electrons can be estimated by using the expression $N_{it} = \frac{C_{ox}(V_{FB}-V_{FB(UV)})}{qA}$ where V_{FB} and $V_{FB(UV)}$ are flat band voltages before applying accumulation bias stress and after UV light exposure to the MOS capacitors respectively. The number density of released trapped charge in hot plate Al_2O_3 sample is ~ $4x10^{12}$ cm^{-2}. The flatband voltage after UV exposure is close to the theoretical value suggesting that most of the trapped electrons within the oxide are released during the UV treatment. These traps are filled again once the sample is biased in accumulation as seen in the final sweep (light blue curve).

The behavior in the all other Al_2O_3 samples is similar regarding the effect of the UV light exposure. The same experiment for ALD Al_2O_3 is shown in figure 5b). As in the hot plate sample electrons are trapped within the oxide under accumulation bias and are not released again unless UV exposure under deep depletion is applied. The main difference here is that electrons are immediately re-trapped within the oxide during the first sweep after UV exposure (dark blue curve). A stretch-out of the CV curve suggests that electrons are recaptured within the oxide as the gate voltage leads the device to accumulation. In contrast, strong accumulation bias is needed to recapture electrons within the hot plate Al_2O_3 (see dark blue curve in Figure 5a).

The possible effect of the UV light is twofold. Firstly, it is possible that the UV photons are "absorbed" by the trapped electrons in the Al_2O_3 resulting in a release of the electrons to the SiC conduction band. Secondly, the UV exposure creates electron hole pairs and the depletion layer shrinks correspondingly. This means that the electric field across the oxide increases which can result in enhanced field assisted emission of electrons from traps within the Al_2O_3 to the SiC conduction band. We cannot distinguish between these two possibilities in this experiment but very similar behavior has been observed for thermal oxides on SiC containing sodium ions [27].

This experiment demonstrates two things. First, the net negative charge observed in the Al_2O_3 layers is not a permanently fixed charge but rather electrons trapped within the oxide which can be released to the SiC using depletion bias and UV exposure. Such net negative oxide charge is reported in ALD grown Al_2O_3 in literature but the charge density is typically an order of magnitude higher than what is observed in this study [9-11]. The negative charge has been attributed to charged ions within the oxide and assumed to be fixed oxide charge but has not been investigated further as done here. Secondly, we have some initial trapping of electrons in the aluminum oxides during growth which is possible to enhance by accumulation bias.

The main results reported here are rather remarkable. Al_2O_3 grown by oxidation of Al on a hot plate has significantly better electrical properties than ALD or RTP grown films. However, electron injection and relatively low breakdown field (5MV/cm) are still parameters that need to be improved in order to use Al_2O_3 dielectrics in SiC MOS technology.

4. Conclusions

We find the Al_2O_3 layer grown by repeated deposition and subsequent low temperature (200°C) oxidation of thin Al layers using a hot plate are more immune to electron injection and have a very low density of traps at the Al_2O_3/SiC interface compared to Al_2O_3 grown by ALD or RTP. Electron injection within the Al_2O_3 during positive bias stress and the release of injected electrons by UV light illumination show that our Al_2O_3 samples do not contain negative fixed charge as frequently mentioned in literature. Breakdown field of the hotplate Al_2O_3 is ~ 5 MV/cm which is higher than of Al_2O_3 samples grown by ALD or RTP but still only half the value obtained in thermal SiO_2 grown on 4H-SiC. It is possible to increase the breakdown voltage of the Al_2O_3 based MOS capacitors by depositing a SiO_2 layer on the top of hot plate Al_2O_3 and maintain low density of interface traps at the Al_2O_3/SiC interface.

Acknowledgements

This work was financially supported by The University of Iceland Research Fund. We also acknowledge support from the Swedish Foundation for Strategic Research (SSF), and the Knut and Alice Wallenberg Foundation (KAW).

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Paper E

Study of near-interface traps in n-type 4H-SiC MOS capacitors from conductance signal under strong accumulation

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manuscript in preparation.

Study of near-interface traps in n-type 4H-SiC MOS capacitors from conductance signal under strong accumulation

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Abstract. We find a clear correlation between the density of near-interface traps (NITs) in MOS capacitors, fabricated on off-axis (0001) and on-axis (11$\underline{2}$0) face n-type 4H- and 6H-SiC with dry oxides, and the strength of a conductance signal observed under strong accumulation. The conductance signal strength in capacitors having dry thermal oxides varies with temperature and can be described by electron capture and emission at NITs at a rate close to the ac test signal frequency. The findings here show that the signal depends on temperature due to thermal emission of electrons from the NITs rather than direct tunneling. However, direct tunneling is also present and is more prominent in samples containing low density of NITs such as oxides made by sodium enhanced oxidation (SEO).

2. Introduction

The great potential of silicon carbide metal-oxide-semiconductor field effect transistors (SiC MOSFETs) for power electronics is hampered due to the presence of traps close to the conduction band of SiC that capture electrons at the interface between the gate oxide and SiC [1-4]. The interface traps are commonly classified into fast interface traps that are located exactly at the oxide/SiC interface and near-interface traps (NITs) or border traps that are located within a tunneling depth of a few angstroms into the gate oxide with energy levels near the SiC conduction band [5,6]. Capacitance and conductance measurements (CV and GV) are the most common methods to determine the quality of insulator/semiconductor interfaces [7]. A frequently observed feature in SiC MOS capacitors is a non-zero conductance when the sample is under strong accumulation bias. The conductance in accumulation increases with frequency and similar behavior has been observed if there is a high series resistance within the MOS capacitor [7]. This behavior in SiC MOS samples was normally attributed to series resistance and was not carefully investigated. However, it was recently reported that this conductance signal stems from tunneling of electrons to and from NITs rather than the series resistance [8]. In this work, we examine the conductance signal for thermally grown silicon dioxide (SiO_2), in different ambient, on (0001) and (1120) face 4H- and (0001) face 6H-SiC and investigate its correlation with NITs.

2. Experimental methods

Off-axis (0001) face 4H-SiC samples are made on commercially available highly nitrogen doped wafers having a 10 µm thick n-type epilayer. The doping concentration in the epilayer was about $1x10^{16}$ cm^{-3} as determined by C-V analysis. A 32 nm thick SiO_2 was formed in dry oxygen at 1240°C for 40 min and a 37 nm oxide was formed in nitrous oxide (N_2O) at 1240°C for 90 min. Another SiO_2 film was made by intentional sodium contamination typically called sodium enhanced oxidation (SEO). In the SEO method, a 100 nm oxide was grown in O_2 ambient at temperature between 1000 and 1240°C and densified in nitrogen ambient at 1000°C for 5 h. This whole oxidation process was performed in alumina furnace tube with a carrier boat made of sintered alumina. The alumina contains trace amounts of sodium which is responsible for increase in oxidation rate and for the reduction of NITs. The on-axis (11$\underline{2}$0) face 4H-SiC sample was oxidized in dry oxygen at 1100°C for 1 h and post annealed in Ar for 1100°C for 1h. The resulting oxide thickness was 71 nm.

In addition, an oxide-nitride (ON) structure was made on off-axis (0001) face 6H-SiC substrate, having highly doped n-type substrate with a nitrogen doped epilayer ($1x10^{16}$ cm^{-3}). ON structure was made by dry thermal oxidation in O_2 at 1150°C for 90 min followed by silicon nitride (Si_3N_4) deposition at 800°C using low pressure chemical vapor deposition resulting in effective oxide thickness of 53 nm. Circular MOS pads were made using Al as a gate metal and the backside contact was also made by Al metallization. In this work to study the nature of interface traps at SiO_2/SiC interface, the CV and GV measurements are performed on 300 µm MOS pads, using Agilent E4980A LCR meter, at different test frequencies, ranging from 1 kHz to 1 MHz, and at different temperatures between 200 K and 400 K.

3. Results

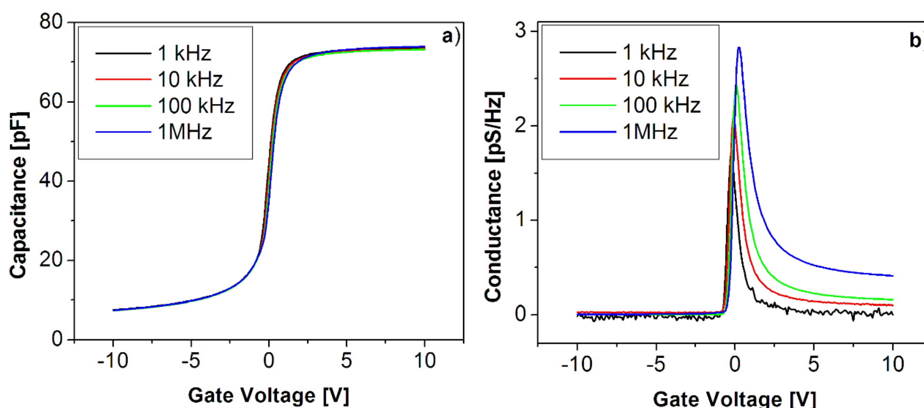

Figure 1. Room temperature CV and GV characteristics of n-type 4H-SiC (0001) MOS capacitor, with dry thermal oxide grown at 1240°C, measured at 1 kHz - 1 MHz.

Room temperature CV and GV spectra, at frequencies between 1 kHz and 1 MHz, of n-type 4H-SiC (0001) MOS capacitor with thermally grown SiO_2 at 1240°C are shown in figure 1. Frequency dispersion in CV characteristics enables us to get an estimate of the distribution of interface traps. A rather small frequency dispersion in

the CV curve (Figure 1a) indicates the reasonable good quality of oxide. In the GV curves (figure 1b) the well-known conductance peak occurs near flatband conditions and is due to response from interface traps near the Fermi level [7]. A noticeable feature in GV curves is non-zero accumulation conductance. This can be due to the impact of series resistance which can give rise to frequency dependence in the measured conductance and has greatest effect in strong accumulation [7]. Series resistance can be determined from standard equivalent circuit of MOS capacitor in strong accumulation. But we found that it is not possible to find a value for the series resistance that can explain the non-zero conductance in figure 1b over all frequencies using the well-known method for such correction [7]. The same applies to all other SiC capacitors that we have investigated so our findings agree with ref. [8] with respect to series resistance. However, the series resistance has a certain impact on the high frequency data (above 100 kHz) as discussed below.

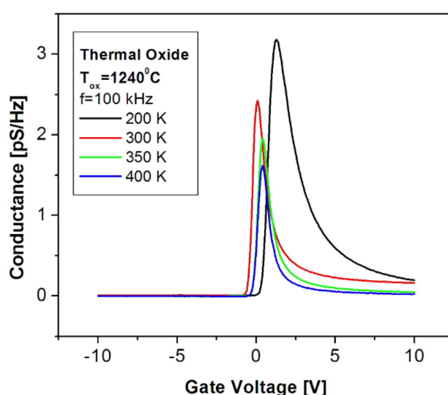

Figure 2. GV curves at 100 kHz of 4H-SiC (0001) with SiO_2 grown in dry O_2 at 1240°C.

Figure 2 shows the typical effect of temperature on the GV curves for capacitors containing dry oxides. The conductance in strong accumulation (10 V) depends on the sample temperature and is in this case maximized at 200 K. In ref [8] no temperature dependence was observed and the signal was therefore attributed to direct tunneling of electrons between NITs and the SiC conduction band. In our studies, we note that the conductance signal exists at all temperatures (between 200 - 400 K) which supports the direct tunneling hypothesis. However, in addition there is a temperature dependent contribution to the conductance signal that indicates thermally activated capture of electrons at the NITs. This is not a surprising result since it is well established that NITs located near the SiC conduction band edge exhibit thermally activated electron capture with very wide range of electron capture cross sections [4,6].

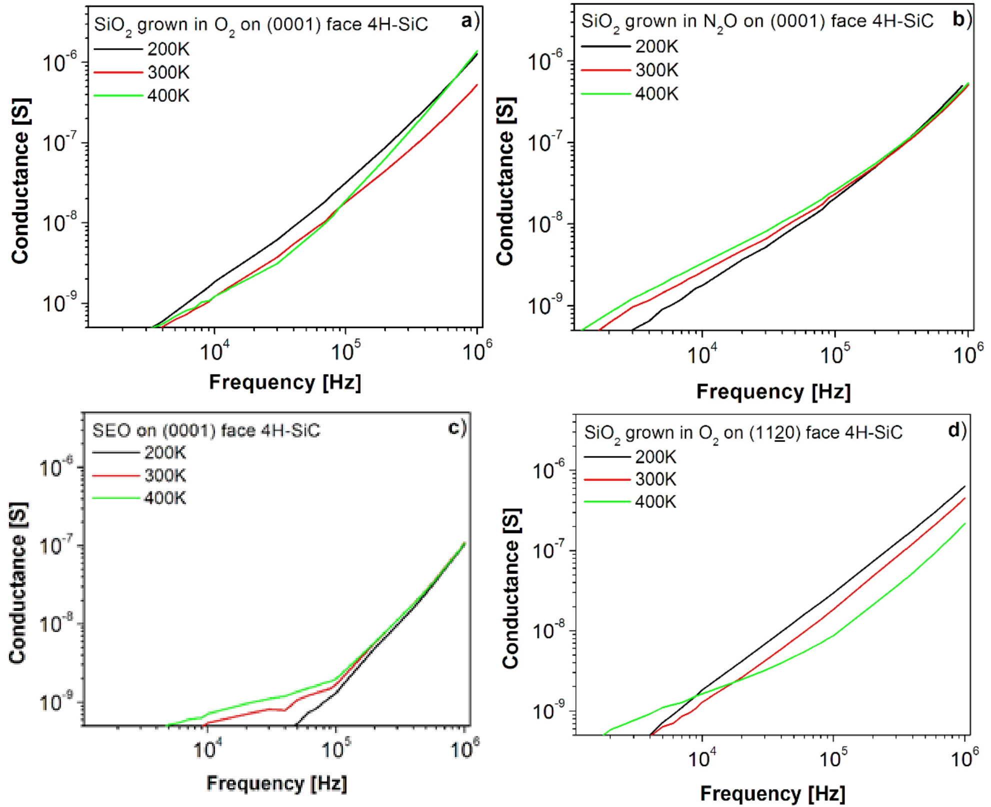

Figure 3. Conductance measured at gate voltage of 9.5V over different frequencies and temperatures for oxide SiO_2 grown on (0001) face 4H-SiC a) in pure O_2 at 1240°C b) in N_2O ambient at 1240°C c) by SEO and for d) oxide grown on (11$\underline{2}$0) face 4H-SiC in pure O_2 at 1100°C.

Figure 3 shows the conductance of thermally oxidized (0001) and (11$\underline{2}$0) face 4H-SiC MOS capacitors at temperatures between 200 K and 400 K corresponding to the gate bias well into accumulation (V_G= 9.5 V). The conductance exhibit temperature dependencies. This suggests that the communication between free carriers (electrons) and NITs is due to temperature dependent mechanism. In figure 3a of typical dry oxide on (0001) 4H-SiC the conductance is maximum at 200 K. There is a steep increase in the conductance profile at 400 K for high frequencies (100 kHz to 1 MHz), this is due to an increase in the series resistance of the sample which is analyzed in the next section. SiO_2 grown on (0001) 4H-SiC in the presence of N_2O gas in figure 3b shows temperature dependent electron trapping at low frequencies while the conductance signal does not vary significantly with temperature for high frequencies. Figure 3c shows that the conductance signal in SEO grown oxide on (0001) 4H-SiC is about an order of magnitude lower than dry oxides grown in presence of O_2 and N_2O. This overall behavior of the conductance with frequency and temperature is very similar to the N_2O oxidized MOS capacitor. The SEO method strongly reduces the number density of interface states near the conduction band of SiC [9]. This suggests that the signal scales with the density of NITs. Figure 3d shows the conductance data for (11$\underline{2}$0) face 4H-SiC with thermal oxide grown in O_2.

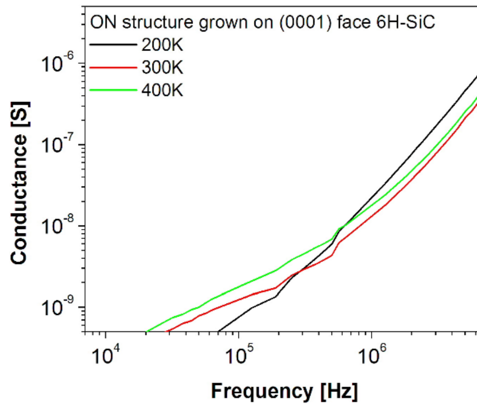

Figure 4. Conductance measured over different frequencies and temperatures for ON structure grown on (0001) face 6H-SiC.

Figure 4 shows the conductance of ON structure grown on (0001) face 6H-SiC as a function of frequency at temperature between 200 K and 400 K. The conductance signal in the ON sample is strongly temperature dependent. At low frequency, the high conductance signal for elevated temperature indicates the presence of deep NITS whose response is of the order of 500 kHz at 400 K. Previous work on 6H-SiC sample with dry oxide grown in O_2 investigated by thermally stimulated current (TSC) technique indicates a high density of NITs very close to the conduction band of 6H-SiC [10].

4. Analysis and Discussion

NITs (or border traps) have been investigated in high-k dielectrics grown on III-V semiconductors [11-13]. Direct tunneling and temperature dependent capture/emission from NITs has been observed [13]. The NITs in very thin dielectric grown on InGaAs are known to have an impact on the accumulation conductance in GV analysis as well as on the accumulation capacitance in CV studies [11,12]. A method to estimate the density of NITs from GV and CV data was reported in Ref. [11]. In that model, the NITs are distributed throughout the oxide and their impact is calculated using an equivalent circuit model adding the incremental contributions of each trap to the total conductance and capacitance of the MOS capacitor. The key parameters required for that model are: (1) oxide capacitance and its thickness, C_{ox} and t_{ox}, (2) fermi level position at the interface, E_f, that directly defines the energy position of detected NITs (3) time constant associated with communication of free carriers between NITs and the semiconductor, τ_o and (4) volume density of NITs in oxide, N_{bt}, at an energy position selected by E_f. In addition, a series resistance, R_s, and conductance by dielectric tunneling leakage, $G_{Ln,}$ was pointed out later [12] since without R_s and G_{Ln} this model did not work very well. In our case the dielectric is thick so the conductance component G_{Ln} is neglected. Furthermore, R_s has strong impact on the high frequency measured conductance but not on the measured capacitance. Like a previous study [13], we also calculated the capacitance and conductance of MOS devices having NITs as a function of frequency and compared them with experimental results.

Firstly, the impact of R_s on the high frequency GV data is observed and extracted by plotting the measured data in the accumulation region, $G_m/\omega C_m^2$, against frequency [12]. As an example, we extracted the R_s value at room temperature for (0001) faced 4H-SiC MOS capacitor with thermally grown SiO_2 in O_2 at a gate voltage from 8V to 10 V. This is shown in figure 5a, the slope of linear regime gives R_s ~1.47×10^{-3} Ω cm^2 over gate area of 7.065×10^{-4} cm^2. The R_s correction of the GV profile for the same MOS capacitor at 100 kHz and 1 MHz is shown in figure 5b. It is clear that the R_s has an impact only at frequencies above 100 kHz (and this also applies to all other samples investigated) and it is in agreement with Ref. [12]. The R_s value at 400 K for the same MOS capacitor is extracted and is found to be 4.58×10^{-3} Ω cm^2. This shows that R_s is in this case temperature dependent and the strong increase in the 400 K conductance profile above 100 kHz in figure 3a is due to an increase in R_s.

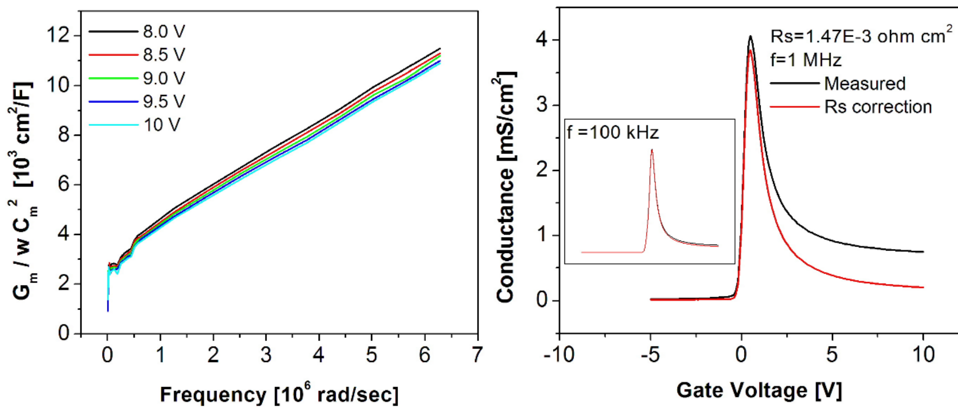

Figure 5. a) $G_m/\omega C_m^2$ is plotted against ω for R_s extraction of Si faced 4H-SiC MOS capacitor with thermally grown SiO_2 in O_2. The extracted R_s is ~ 1.47×10^{-3} Ω.cm^2. b) R_s corrected GV profile of same thermal oxide at 1 MHz. R_s has minor impact on GV curve at 100 kHz as shown in inset.

We have used the model mentioned in Ref. [11] to estimate the N_{bt} based on the conductance data in accumulation, taking also into account the possible effect of R_s [12]. In the simulations presented here the energy level of the NITs is assumed to be at the 0.1 eV above the conduction band position of SiC. The exact energy level position does not have a significant impact on the overall result. An example of the results of such a fitting procedure are shown in figure 6.

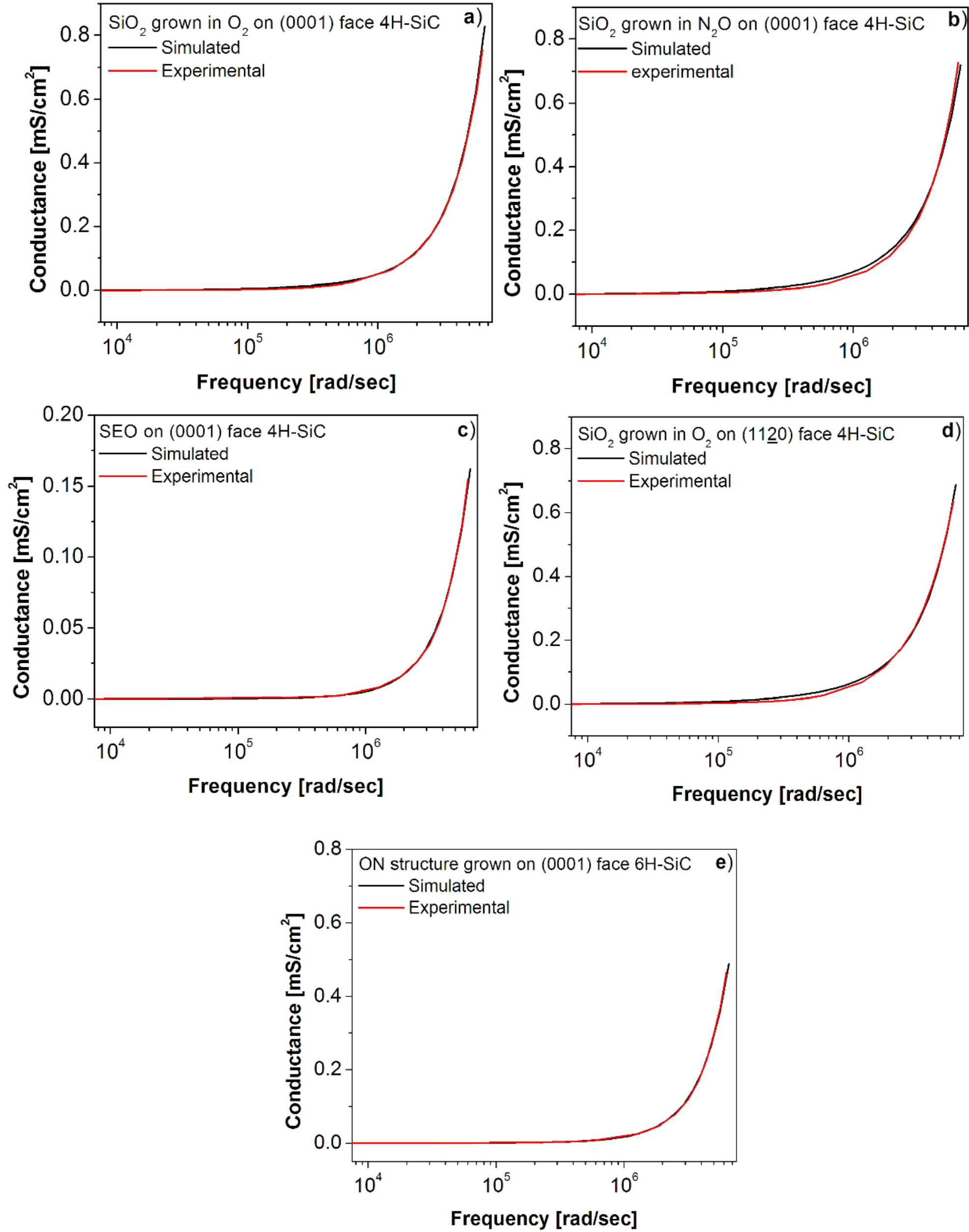

Figure 6. Simulated and room temperature experimental conductance data for SiO_2 grown on (0001) face 4H-SiC a) in pure O_2 and b) in N_2O ambient, c) by SEO, d) for SiO_2 grown on (11$\underline{2}$0) face 4H-SiC in pure O_2 and for e) ON structure grown on (0001) face 6H-SiC at gate voltage of 9.5 V.

Figure 6 shows the simulated and room temperature experimental conductance profiles of SiO_2 MOS capacitors at gate voltage of 9.5 V. The key fitting parameters are N_{bt} and R_s. The R_s value in these samples is in the range of 1- 4×10^{-3} $\Omega.cm^2$. The time constant is taken 10^{-9} sec. The extracted active N_{bt} at room temperature is ~

4×10^{17} cm^{-3} and ~ 5×10^{18} cm^{-3} for SiO_2 grown in SEO and N_2O ambient respectively. The dry oxides grown in O_2 on (0001) and (11$\underline{2}$0) face 4H-SiC have almost same value of extracted N_{bt} of ~ 2×10^{19} cm^{-3} at 300 K. The ON structure on (0001) face 6H-SiC sample has ~ 1.3×10^{18} cm^{-3} volume density of NITs. The extracted value of N_{bt} by fitting simulated and experimental conductance data shows that SEO significantly reduces the density of NITs. Simulation model has been extended further to obtain the depth profiles of NITs within the oxide as well as their location in energy by considering the temperature and frequency dependent response of NITs located close to semiconductor conduction band edge [13]. Using that method [13] and by considering the area of capture cross section of traps in ~ 10^{-17} cm^2, the active depth of the NITs (located at 0.1 eV above the conduction band position of SiC) in dry oxide is of the order of ~ 1 nm. In this work, we assume the depth profile across 1 nm to be constant. This then gives the surface density of NITs, S_{bt}, in the $2\text{x}10^{12}$ cm^{-2} range for dry oxides grown in O_2 on (0001) and (11$\underline{2}$0) face 4H-SiC, about $4\text{x}10^{10}$ cm^{-2} for the SEO oxide and ~ 5×10^{11} cm^{-2} for oxide grown in N_2O on (0001) 4H-SiC. The ON structure on (0001) face 6H-SiC sample has S_{bt} of ~ 1.3×10^{11} cm^{-2}. These values are close in magnitude as shown in table 1 to previous estimated values of NITs in identical samples using a method called thermal dielectric relaxation current (TDRC) [9,10,14,15]. More simulations are needed to test this model further, including the effect of temperature, but it provides an estimate of NITs which agrees with more elaborate experimental methods.

Table 1. Comparison of surface density of NITs extracted by simulation model and by TDRC

SiC MOS device	S_{bt} by simulation model	S_{bt} by TDRC
(0001) faced 4H-SiC MOS device with oxide		
grown in O_2 ambient	~ $2\text{x}10^{12}$ cm^{-2}	~ $3\text{x}10^{12}$ cm^{-2}
grown in N_2O ambient	~ 5×10^{11} cm^{-2}	~ 1×10^{12} cm^{-2}
grown by SEO	~ 4×10^{10} cm^{-2}	~ 1×10^{11} cm^{-2}
(0001) faced 6H-SiC MOS device with oxide		
grown in O_2 ambient	~ 1×10^{11} cm^{-2}	~ 3×10^{11} cm^{-2}
(11$\underline{2}$0) faced 4H-SiC MOS device with oxide		
grown in O_2 ambient	~ $1.6\text{x}10^{12}$ cm^{-2}	~ $2\text{x}10^{12}$ cm^{-2}

4. Conclusions

We find that the conductance signal in n-type 4H- and 6H-SiC MOS capacitors in accumulation can be explained by a combination of tunneling and thermally activated capture and emission of electrons between NITs and the SiC conduction band. It is possible to estimate the density of NITs from the conductance data using models

previously developed for studies of high-k dielectrics and the extracted data is in a reasonable agreement with estimates of NITs using TDRC [9-15]. Further studies of these conductance signals are needed to verify the usefulness of this approach to investigate NITs.

Acknowledgements

This work was financially supported by University of Iceland Research Fund.

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