Detection of very fast interface traps at the SiC/insulator interface using different electrical characterization techniques

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Faculty of Physical Sciences
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2023

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Dissertation submitted in partial fulfillment of a
Philosophiae Doctor degree in Physics

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Bibliographic information:
Arnar Már Viðarsson, 2023, *Detection of very fast interface traps at the SiC/insulator interface*, PhD dissertation, Faculty of Physical Sciences, University of Iceland, 132 pp.

ISBN 978-9935-9630-6-2

Printing: Háskólaprent
Reykjavik, Iceland, 2023

True knowledge is knowing the extension of one's ignorance.
- Confucius

This thesis is dedicated to my loving family.

Abstract

The semiconductor silicon carbide (SiC) might be the key to next-generation of power electronic devices. Its favourable material properties can outperform existing silicon (Si) devices enabling better energy efficiency in power electronics. However, the SiC metal-oxide-semiconductor-field-effect-transistors (MOSFETs) made using silicon dioxide (SiO_2) as the gate oxide forms a poor interface to the SiC, resulting in low inversion channel-carrier mobility which prevents fabrication of low voltage devices (< 650 V).

In this study we investigate electron emission from interface defects at the SiC/dielectric interface using various electrical analysis methods at cryogenic temperatures. Such interface defects limit the electron mobility in SiC MOSFETs. The experimental methods used include capacitance voltage measurements (CV), conductance spectroscopy and thermal dielectric relaxation current (TDRC). These studies reveal a very fast electron trap that can be observed at cryogenic temperatures using CV and conductance spectroscopy. This trap has been labelled as NI. The NI trap shows up as a frequency dispersion in CV at high frequencies that gets larger as the sample is cooled to lower temperatures, and as a conductance peak in conductance spectroscopy that appears when bias corresponding to weak depletion is applied.

We observe the NI trap in SiO_2 that has been made using dry oxidation, dry oxidation followed by annealing in N_2O or pure NO at high temperatures, aluminium nitride (AlN) and aluminium oxide (Al_2O_3). It was hypothesized that the NI trap was located inside the SiO_2 with energy levels close to the SiC conduction band edge and the conductance signal was due to electron tunnelling to and from the defect. The observation of the NI trap in both AlN and Al_2O_3 suggests that the NI trap is not a property of the dielectric but rather related to the surface properties of the SiC.

However, in samples were the SiO_2 made using sodium enhanced oxidation (SEO) the NI trap are absent both in CV and conductance spectroscopy measurements. MOSFETs made using SEO show improved inversion channel-carrier mobility of about 3 times higher than in NO annealed oxides that are used in commercial SiC MOSFETs. This suggests that electron trapping in NI trap is responsible for poor inversion channel mobility in SiC MOSFETs.

Keywords: Silicon Carbide (SiC), Silicon Dioxide (SiO_2), Aluminium Nitride (AlN), Aluminium Oxide (Al_2O_3), High-κ Dielectrics, High Power Electronics, Metal-Insulator-Semiconductor (MIS) Capacitor, Metal-Oxide-Semiconductor (MOS) Capacitor, Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET), Capacitance Voltage (CV), Conductance Spectroscopy, Thermal Dielectric Relaxation Current (TDRC)

Útdráttur

Aflrafeindatæknin í dag byggir að miklu leyti á rafsviðssmárum (e. MOSFET) sem gerðir eru í hálfleiðaranum kísli (Si). Sú tækni hefur verið bestuð undanfarna áratugi og nú er svo komið að það eru efniseiginleikar kísilsins sem takmarka straumgetu og spennuþol þessara íhluta. Á síðustu árum hafa hins vegar komið fram á sjónarsviðið nýir smárar sem gerðir eru í hálfleiðaranum kísilkarbíð (SiC) sem hafa betri nýtni en hefðbundnir kísilsmárar og leiða til umtalsverðs orkusparnaðar. Fram að þessu er þó einungis hægt að nota SiC smárana við mjög háar spennur ($\geq$650 V). Megnið af þeim rásum sem notaðar eru í aflrafeindatækni vinna hins vegar við spennur á bilinu 300-600 V og þar eru SiC smárarnir ekki samkeppnishæfir. Ástæðan er ekki tengd efniseiginleikum kísilkarbíðsins heldur því hvernig samskeyti SiC myndar við einangrandi efnið kísildíoxíð (SiO_2) sem nauðsynlegt er til að stýra smáranum. Straumgeta smárans takmarkast af því að veilur á SiC/SiO_2 samskeytunum hremma rafeindir sem eru á leið í gegnum smárann sem veldur því að straumurinn er um þrefalt lægri en búast má við ef samskeytin eru gallalaus. Reynt hefur verið að leysa þetta vandamál síðustu 20 árin en ekki tekist enn sem komið er.

Í þessu verkefni er skoðuð rafeindalosun frá veilum á skilum SiC/einangrara með notkun ýmsa rafgreiningaraðferða við mjög lág hitastig. Þessar aðferðir eru rýmdar-spennumælingar (CV), leiðnimælingar og hitastigs örvunar straummælingar (TDRC). Þessar mælingar sýna mjög hraða rafeinda veilu sem hægt er að skoða við mjög lág hitastig. Þessi veila hefur verið nefnd NI. NI veilan kemur fram sem tíðni dreifing í CV mælingum við háar tíðnir sem vex með lækkandi hitastigi, og sem toppur í leiðnimælingu við lágt hitastig.

NI veilan sést í SiO_2 sem hefur verið búið til með þurroxun, í þurroxíði sem hefur verið bakað með hreinu N_2O eða NO gasi við há hitastig, í álnítríði (AlN) og í áloxíði (Al_2O_3). Til þessa hefur verið gert ráð fyrir að NI veilan væri staðsett inní SiO_2 með orkustig nálægt leiðniborðanum og að leiðnimerkið væri vegna smugs til og frá þeirri veilu. Að NI veilan greinist í AlN og Al_2O_3 bendir til að veilan sé ekki eiginleiki SiO_2 einangrarans heldur tengist SiC yfirborðinu.

Hins vegar, ef notað er SiO_2 búið til með natríumaukinni oxun (SEO) sem einangrari þá er NI veilan hvergi sjáanleg bæði í CV og leiðnimælingum. MOSFETar gerðir með SEO oxun sýna einnig aukinn hreyfanleika rafeinda sem er um 3 sinnum hærri en í NO MOSFETum sem nú eru notaðir í aflrafeindatækni. Þetta bendir til þess að NI veilan sé ábyrg fyrir lágum hreyfanleika rafeinda í SiC MOSFETum.

Lykilorð: Kísilkarbíð (SiC), Kísil Díoxíð (SiO_2), Álnítríð (AlN), Áloxíð (Al_2O_3), Hátt-κ Einangrarar, Háorku Íhlutir, Hálfleiðara Þéttar (MIS/MOS), Rafsviðs Smárar (MOSFET/MISFET), Rýmdar Spennu Mælingar (CV), Leiðni Mælingar, Hitastigs Örvunarstraum Mælingar (TDRC)

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List of Appended Papers

I **Near-Interface Trap Model for the Low Temperature Conductance Signal in SiC MOS Capacitors With Nitrided Gate Oxides.**

J.R. Nicholls, A.M. Vidarsson, D. Haasmann, E.Ö. Sveinbjörnsson, S. Dimitrijev

IEEE Transactions on Electron Devices Vol. **67**, Issue 9, 3722-3728, 2020.

II **A method for characterizing near-interface traps in SiC metal–oxide–semiconductor capacitors from conductance–temperature spectroscopy measurements.**

J.R. Nicholls, A.M. Vidarsson, D. Haasmann, E.Ö. Sveinbjörnsson, S. Dimitrijev

Journal of Applied Physics **129**, 054501 2021.

III **Observation of Fast Near-Interface Traps in 4H-SiC MOS Capacitors Using Capacitance Voltage Analysis at Cryogenic Temperatures.**

A.M. Vidarsson, J.R. Nicholls, D. Haasmann, S. Dimitrijev, E.Ö. Sveinbjörnsson

Materials Science Forum **1062**, 288-292, 2022.

IV **Detection of near-interface traps in NO annealed 4H-SiC metal oxide semiconductor capacitors combining different electrical characterization methods.**

A.M. Vidarsson, J.R. Nicholls, D. Haasmann, S. Dimitrijev, E.Ö. Sveinbjörnsson

Journal of Applied Physics **131**, 215702, 2022.

V **Passivation of very fast near-interface traps at the 4H-SiC/SiO_2 interface using sodium enhanced oxidation**

A.M. Vidarsson, D. Haasmann, S. Dimitrijev, E.Ö. Sveinbjörnsson

Accepted for publication in Materials Science Forum, 2023.

VI **Improvement of Channel Mobility in 4H-SiC MOSFETs correlated with Passivation of Very Fast Interface Traps Using Sodium Enhanced Oxidation**

A.M. Vidarsson, D. Haasmann, S. Dimitrijev, E.Ö. Sveinbjörnsson

Manuscript submitted for publication.

VII **Observations of very fast traps at the SiC/high-κ dielectric interface**

A.M. Vidarsson, A.R. Persson, J.T. Chen, D. Haasmann, J.U. Hassan, S. Dimitrijev, N. Rorsman, V. Darakchieva, E.Ö. Sveinbjörnsson

Manuscript in Preparation.

Acknowledgments

I want to thank my supervisor Professor Einar Ö. Sveinbjörnsson for giving me the opportunity to pursue my PhD. degree. Which I would probably never have done without him asking me if I wanted to pursue a PhD back in 2018. Our conversations, that usually started on the latest measurement results but went off on a tangent quite frequently, and before you know it a hour or two have passed, have been a great fun. He has been a great mentor and a friend. He gave me the opportunity to have free hands to test and explore on my own but always keep in mind his catchphrase "Murphy never sleeps".

I want to thank Dr. Rabia Y. Khosa for her guidance in my masters studies back in 2016 to 2018 and in the beginning of my PhD studies.

I would like to thank my colleagues at VR3 for the very entertaining conversation we have had at lunch time. If the phrase "Hláturinn lengir lífið (e. Laughter prolongs life)" is true I think I have added few decades to mine.

Finally, I would like to thank my mother, father and brother for the support they have given me thought the past 12 years when I first started my journey. I would never have been able to do this without your support.

Chapter 1

Introduction

Silicon carbide (SiC) is one of the best semiconductor candidates for the next generation of power devices in the 21st. century. This is due to its large energy band gap, high thermal conductivity, high electric breakdown field and high electron saturation velocity. These properties are ideal for electrical components that require high power, high frequency and/or operate at high temperatures. The metal-oxide-semiconductor-field-effect-transistor (MOSFET) is the basic building block of logic in modern electronic technology and is used in most electrical devices. With the push to renewable energy sources, electric personal vehicles and public transportation the demand for electrical components that can operate at high power has increased significantly and SiC-MOSFETs have been increasing in demand since the first SiC-MOSFET from Cree in 2011 [1].

However, the commercial production of SiC-MOSFETs comes with its share of challenges that need to be overcome. One of the most significant challenges is the poor inversion channel carrier mobility between the drain and the source. Though the process of growing a silicon dioxide (SiO_2) on top of the SiC is relatively easy the quality of the SiC/SiO_2 interface is rather poor. SiC has quite a few polytypes but the 4 hexagonal (4H) is the most common one used in commercial devices. The current solution to the poor mobility in commercial devices has been to post anneal the SiO_2 in pure nitric oxide (NO) at high temperatures. This process improves the carrier mobility of SiC-MOSFETs from about 1 cm^2/Vs to 35 - 50 cm^2/Vs. However, even with these improvements the electron channel mobility in SiC is still far from its theoretical limit. At the time of writing the available blocking voltages in SiC-MOSFETs are 650 V and above. Attempts to fabricate devices with lower blocking voltages have not been successful as the high on-resistance of the SiC-MOSFET due to the low mobility reduces the efficiency of the device to unacceptable limit.

In this work the 4H-SiC/insulator interface is studied using metal-insulator-semiconductor (MIS) capacitors using a variety of different electrical characterization methods at room- and cryogenic temperatures.

Chapter 2

The Silicon Carbide Semiconductor

2.1 The 4H-SiC Crystal Structure

Silicon carbide has many forms of stable crystal structures or polytypes. The most common one in applications is the 4 hexagonal (4H) polytype which is used in this study.

The SiC crystal structure is formed by every silicon atom surrounded by four carbon atoms and every carbon atom is surrounded by four silicon atom forming a tetrahedral structure as seen in figure 2.1 a). The 4 in the 4H-SiC refers to the stacking order of the atom bi-layers in 4H-SiC crystal, meaning that it takes 4 bi-layers to repeat the stacking pattern as seen in figure 2.1 b) and is noted as ABCBABCB.... The 4H-SiC crystal has equal number of hexagonal and cubic bonds that are often refereed to as h- and k-cites and are marked in figure 2.1 b). When the SiC crystal is doped the dopant atoms will replace either an atom located at h-site or k-site and these dopant atoms will have slightly different ionization energies depending on the lattice position.

The main crystal face used in manufacturing of modern commercial SiC MOSFETs devices is the (0001) face also referred to as the Si-face. Most production wafers are grown on axis but are cut with a 4° off axis angle to the Si-face. The 4° off axis cut is mainly due to the growth methods used to grow the epitaxial layer [2], [3]. The crystal vectors are shown in figure 2.2 a) and the most relevant faces in figure 2.2 b). The $(11\bar{2}0)$ or the a-face is of particular interest as it has shown promising results for lower interface state density compared to the Si-face and higher inversion channel mobility in MOSFET structures [4]–[6]. However, we did not test a-face structures in this study. All samples used in this study are fabricated on the Si-face of the SiC wafer.

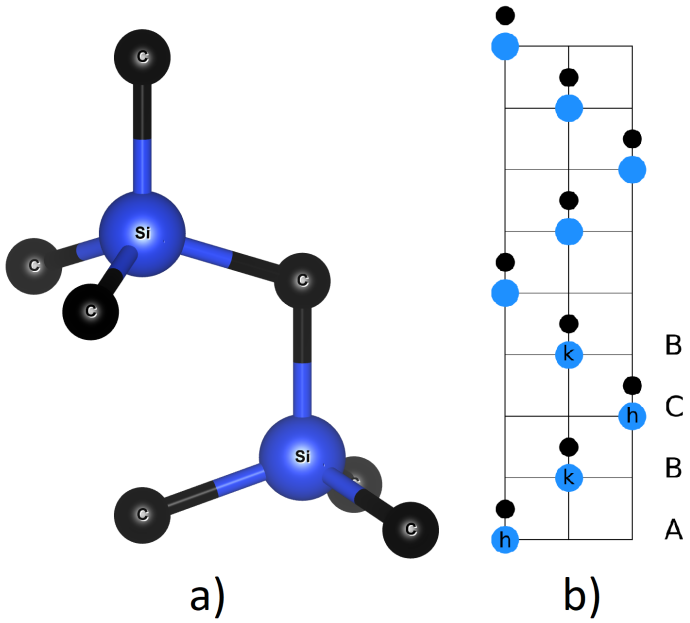

Figure 2.1: a) 4H-SiC atom structure. b) Atom stacking of the 4H-SiC crystal.

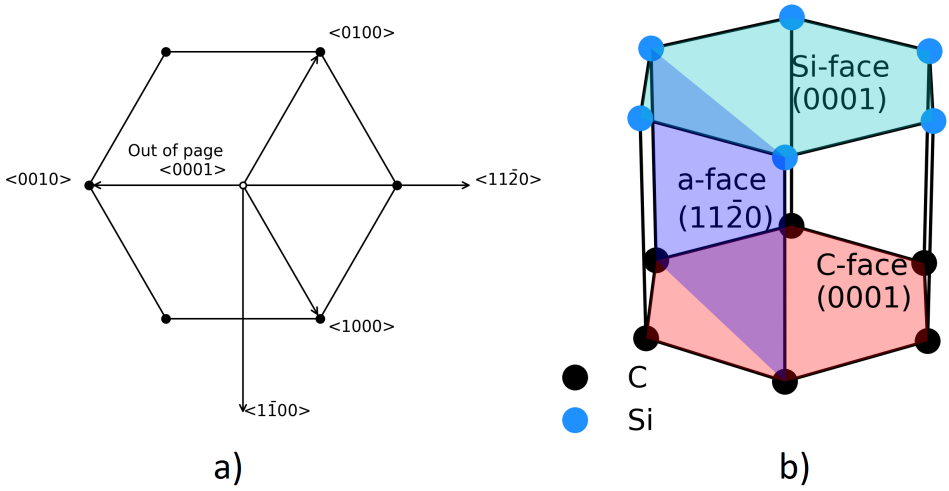

Figure 2.2: a) Top view of the crystal vector. b) <1000>, <0100> and <0010> are the basal plane of the SiC crystal.

2.2 Physical Properties of 4H-SiC

Table 2.1 lists the most relevant physical properties of the 4H-SiC semiconductor. In this study only n-type substrates doped with nitrogen dopant atoms are used to fabricate the MOS capacitors while p-type (epilayer) substrates were used to fabricate MOSFETs. 4H-SiC is more isotropic than the other polytypes thus making it more suitable than the other SiC polytypes for high-power, high-frequency and high temperature devices. The physical parameters of particular interest are the wide energy bandgap, high thermal conductivity and high breakdown field.

Physical Property	Value
Energy Bandgap	3.26 eV
Dielectric constant ϵ_s	9.7
Thermal Conductivity	5.0 W/cm K
Lattice Constant a	3.073 Å
Lattice Constant c	10.05 Å
Electron Effective Mass m_e/m_0	0.45
Hole Effective Mass m_h/m_0	0.66
Bulk Electron Mobility $\mu_e \perp$ c	800 cm^2/Vs
Bulk Electron Mobility $\mu_e \parallel$ c	880 cm^2/Vs
Bulk Hole Mobility	60 cm^2/Vs
Saturation Velocity	2×10^7 cm/s
Breakdown Field	2.2 MV/cm
Ionization Energy of N h site	40 meV
Ionization Energy of N k site	80 meV

Table 2.1: Table listing the main physical properties of the 4H-SiC semiconductor at room temperature with doping concentration of $10^{16} cm^{-3}$ [7].

2.3 SiC MISFET Power Devices

With the modern world shifting its attention more to renewable energy sources there is demand for more efficient ways of utilizing that energy. SiC high power devices have increasingly become more relevant as they perform more efficiently at high power and temperature, than their Si based

counterparts [8].

Metal-insulator-semiconductor-field-effect-transistor (MISFET) device is a three to four terminal switching device. Note that here we use insulator, I in the acronym, as in this study we investigate not only oxides but also other dielectric that is not an oxide. The terminals are drain, source, gate and body/p-well. However, the p-well contact is often shorted to the source terminal. To keep things simple we will only focus on the three terminal device here that uses the (0001) face for its channel. Other geometric structures of power devices exist and are actively studied such as the V- and U-shaped trench that utilize the $(0\bar{3}3\bar{8})$ and $(11\bar{2}0)$ faces respectively. Figure 2.3 shows a diagram of an n-channel MISFET and a simplified n-type MIS capacitor. MIS capacitors are used to study the quality of the interface, defects, and gate integrity and stability. The principle of operation of a

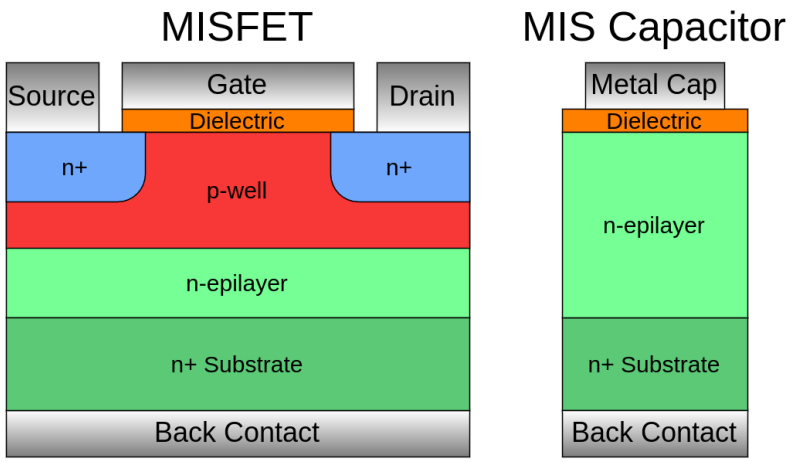

Figure 2.3: Left: Diagram of n-channel MISFET showing the three terminals and flow of current thought the device. Right: n-type MIS capacitor diagram representing the channel of the MISFET structure.

MISFET is in a sense rather simple. It works as a switch where the applied voltage to the gate controls the on/off state. For n-channel MISFET, the drain and source are n-type and the channel is p-type. This forms an energy barrier between the drain and the source as figure 2.4 shows. Thus when voltage is applied between the drain and the source the barrier prevents electrons from flowing from source to drain; the off state. Applying voltage to the gate will lower the energy barrier between the drain and the source allowing electrons to flow from source to drain; the on state. When voltage is applied to the gate, electrons accumulate at the interface forming the channel

between the drain and source. The quality of the semiconductor insulator interface is a big factor when it comes to the efficiency of the MISFET. Poor quality interface results in electron scattering along the channel or electron capture by defects/traps resulting in reduction of electron mobility and higher resistance in the channel when the device in the on state, called on-resistance ($R_{DS_{on}}$). Modern power SiC-MOSFETs can be bought with blocking voltage of 650 V and above. However, the poor channel mobility and high $R_{DS_{on}}$ has prevented the development of devices with lower blocking voltage as the efficiency is unacceptably low for such devices.

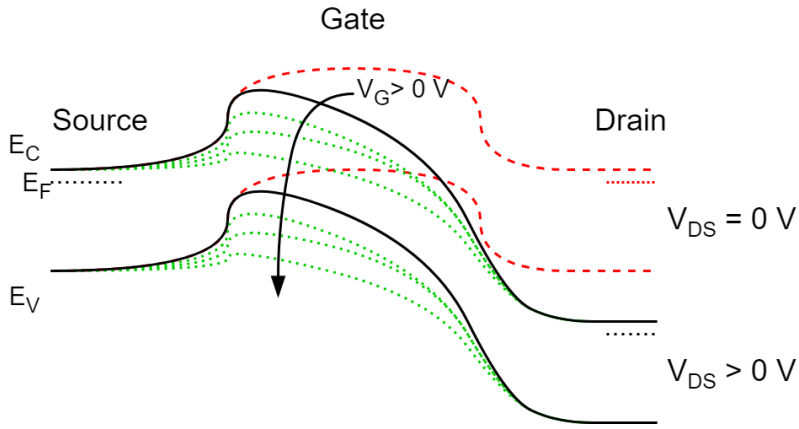

Figure 2.4: Simple energy band diagram of an n-channel MISFET.

Chapter 3

The SiC/Insulator Interface

When fabricating a MISFET device, the gate dielectric has to be grown or deposited to form the channel region of the device. When this is done defects can be introduced at the SiC/dielectric interface. Those defects have been called traps and can be of many different types. Traps located at the SiC/dielectric interface are called interface traps, while traps located 1-5 nm from the interface into the dielectric are called near-interface traps (NITs). Fixed charge and mobile charge can also be present inside the dielectric [9]–[12]. Recent studies of SiC MOS capacitors have also shown existence of a very fast trap that has been given the notation NI [13]. It has been speculated that the NI signal is due to tunnelling to and from traps located 1-2 nm from the SiC/dielectric interface very close to the SiC conduction band edge [14]. Modern SiC high power devices are made using silicon dioxide (SiO_2) post annealed in nitric oxide (NO) which reduces the density of oxide interface traps while the density of NI traps is enhanced [13]. Recent studies have proposed using high-κ dielectrics such as aluminium nitride (AlN) and amorphous aluminium oxide (Al_2O_3) for improvements to the SiC/dielectric interface. High-κ dielectrics also allow the designers of MOSFETs to have the dielectric thicker therefore lowering the risk of gate leakage and/or lower the voltage needed to create the inversion layer in the MOS structure. Figure 3.1 shows the valence- and conduction-band offsets of those dielectrics to 4H-SiC. The band offset between the SiC and the dielectric defines the barrier for injection of holes or electrons into the dielectric bands. The conduction band offset tends to be smaller than the valence band offset. Thus choosing a dielectric with sufficiently large band offset (>1 eV for both valence- and conduction bands) is one of the key criteria for low leakage current [15].

3.1 The SiC/SiO_2 Interface

The most common way to form an insulating dielectric for MOS structure is dry oxidation of SiC using high temperature (1100 - 1300°C) in O_2 ambient

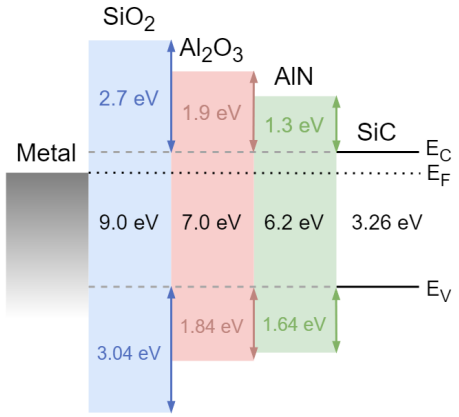

Figure 3.1: Simple illustration of the valence- and conduction-band offsets of SiO_2, AlN and Al_2O_3 to the 4H-SiC valence- and conduction-band edges assuming $\phi_{ms} = 0$ eV [16], [17].

to oxidize the SiC surface resulting in SiO_2 growth following the chemical reactions [18]

$$SiC + \frac{3}{2}O_2 \rightleftharpoons SiO_2 + CO$$

$$SiC + O_2 \rightleftharpoons SiO_2 + C.$$

Additionally, there are secondary reactions that determine the equilibrium at the reaction surface

$$SiC + 2CO \rightleftharpoons 3C + SiO_2$$

$$2C + O_2 \rightleftharpoons 2CO.$$

For the most part the carbon is removed from the interface as CO or CO_2. However, it is believed that carbon does accumulate at the SiC/SiO_2 interface forming carbon clusters or carbon dangling bonds [19]–[21] that cause high density of interface traps resulting in poor channel mobility in SiC MOSFETs, in best cases up to 5 cm^2/Vs [22]. Growing the oxide at higher temperatures reduces the density of interface traps somewhat, but not sufficiently to solve the problem. Studies have shown that growing a very thin oxide layer at the SiC interface does improve in some cases the quality of the interface and reduces the density of interface traps, though the thin film is often grown as a part of a dielectric stack such as a SiO_2/Al_2O_3 stack [23].

Other methods to form the SiC/SiO_2 interface are chemical vapor deposition (CVD) or atomic layer deposition (ALD) of SiO_2. By depositing the SiO_2 instead of thermally growing it, the SiC is not consumed in the reaction

thus minimizing the formation of carbon clusters but dangling bonds at the interface might still form.

SiO_2 is by far the most studied dielectric for SiC power devices and thus there have been many attempts to improve the SiO_2/SiC interface, gate integrity and inversion channel mobility. Some of those methods are summarized below.

- High Temperature Oxidation: Oxidation at a very high temperature. Studies have shown that oxidizing at high temperatures (>1200°C) lowers the density of interface traps [24]–[26]. However, this reduction in density is not substantial.
- Deposition: Depositing the dielectric with ALD before high temperature nitridation. Such studies show reduction in density of interface traps and improved channel mobility [27], [28].
- N_2O anneal: Oxide grown/deposited followed by annealing in N_2O ambient at high temperature or direct oxide growth in N_2O ambient at high temperature [29]. Such oxides contain lower density of interface traps than dry oxides but NO grown oxides produce higher mobility.
- NO/N_2 anneal: Oxide grown/deposited followed by anneal in pure NO or N_2 at high temperature (>1200°C) or oxide grown in pure NO ambient at high temperature [30]–[32].
- H_2 Etching: Before the oxide is grown/deposited the epilayer is etched in H_2 gas then the oxide is grown by thermal oxidation or oxide deposition followed by annealing in NO. Recent studies have reported mobility up to 80 cm^2/Vs [33].
- Sodium Enhanced Oxidation (SEO): Oxide is grown in the presence of sodium, this results in very fast oxide growth, very low D_{it} and high channel mobility of about 150 cm^2/Vs [34], [35]. However, sodium is not a desirable element to have in the oxide since the sodium ion is loosely bound at the interface. If the sample is stressed or heated the sodium ion will depart from the interface leaving a deep trap that significantly shifts the threshold voltage [36].
- Doping the gate oxide: Using phosphorus, boron, rubidium, caesium, strontium or barium to dope the gate oxide have shown promising results for mobility but insufficient reliability [12], [37], [38].
- Using Other Crystal Faces: The $(11\bar{2}0)$ and $(1\bar{1}00)$ have shown promising results even when using normal wet oxidation and very high mobility

of over 100 cm^2/Vs is reported when combined with H_2 etching and NO annealing [4]–[6]. They are made either on wafers that are $(11\bar{2}0)$ or $(1\bar{1}00)$ on the topside of the wafer, making a planar device, or by etching down and making a vertical trench on the (0001) face, where the oxide is then grown/deposited into and the channel is on the vertical $(11\bar{2}0)$ or $(1\bar{1}00)$ faces [39].

Most commercial devices use the post NO/N_2 annealing process as it has shown to be the most reliable method that gives reasonable results for channel mobility, gate integrity and reliability.

3.2 The SiC/Al_2O_3 Interface

The aluminium oxide insulator is commonly made using ALD [16], [40]–[44], chemical vapor deposition (CVD) [45], hot plate deposition [46] or by sputtering [47] either with radio frequency (RF) where the sputter target is Al_2O_3 or reactive sputtering where the sputter target is Al and O_2 is used as a reactive gas in the process. All of these growth methods form an amorphous oxide layer provided the processing temperature is lower than 350°C [48]–[50]. Alone Al_2O_3 suffers from charge injection [42] and high gate leakage current thus a thin SiO_2 layer is sometimes grown before depositing the Al_2O_3 forming a stack. The other alternative is to deposit SiO_2 on top of the Al_2O_3 but the temperature must be kept low (<350°) to avoid crystallization of the Al_2O_3 which results in excessive leakage through grain boundaries [16], [43]. The peak mobility reported thus far has been in the range from 50 - 250 cm^2/Vs [45], [51]. In this study we performed measurements on Al_2O_3 grown using a hot plate method where thin Al film (1-2 nm) is deposited using e-beam then the sample is placed on a 200 °C hot plate in atmospheric ambient for 5 min. This is repeated 12 times resulting in a 15 nm thick amorphous Al_2O_3. A scanning transmission electron microscopy (STEM) image of the SiC/Al_2O_3 is shown in figure 3.2. The figure shows the periodic atom layer stacking of the 4H-SiC and the Al_2O_3 appears dark as it is amorphous.

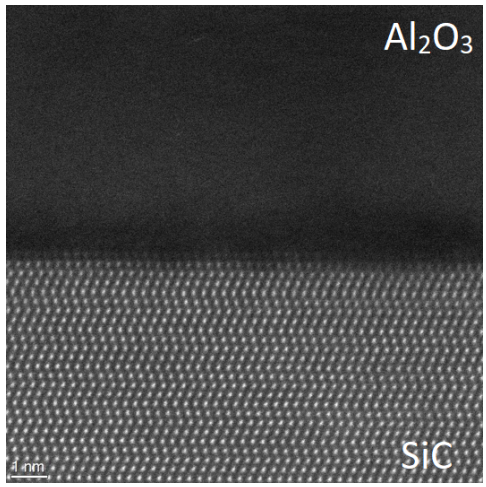

Figure 3.2: STEM image of the SiC/Al_2O_3 interface where the Al_2O_3 was grown using the hot plate method. The image shows the 4H-SiC periodic atomic structure and the amorphous Al_2O_3 that appears dark. Credit to Dr. Axel Persson, Linköping University, see paper 7.

3.3 The SiC/AlN Interface

Aluminium nitride is an interesting dielectric for SiC MIS devices as it has very closely matched a lattice constant parameter to SiC, with $a \approx 3.1106 - 3.1120$ Å [52]–[54] when forming a 2H-AlN crystal, which is about 1.2% mismatch to that of SiC. AlN is often used as a buffer layer on SiC to grow gallium nitride (GaN) on top of the AlN [55]–[57]. Not many studies have been done using AlN as gate dielectric for SiC devices but studies show some promising results [58]–[61]. In this study we use AlN nitride grown using metal-organic chemical vapor deposition (MOCVD) at 1100°C forming a 2H-AlN crystal. Figure 3.3 shows the 4H-SiC periodic stack transitioning into the 2H-AlN layer stacking.

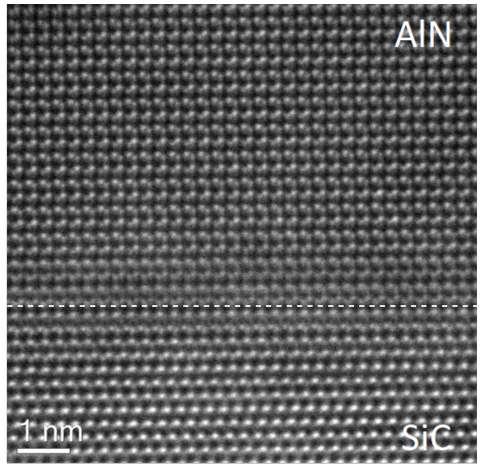

Figure 3.3: STEM image of the SiC/AlN interface grown using MOCVD. The images shows the 4H-SiC atomic structure transitioning into the 2H-AlN. THe dashed line shows the transition layer from 4H-SiC to 2H-AlN. Credit to Dr. Axel Persson, Linköping University, see paper 7.

Chapter 4

Experimental methods

In this work a variety of electrical characterization methods are used to characterize the SiC/insulator interface. The measurements are performed on MIS capacitors that are made by either oxidizing SiO_2, depositing AlN or Al_2O_3 on a 4° off axis 4H-SiC wafers with deposited aluminium on top of the dielectric and make contact pads with known area using lithography. All measurements were done in a Leybold closed loop helium cryostat where temperature is controlled and monitored by a Lakeshore 311 temperature controller.

The MIS structure can be modelled as a capacitor and resistor circuit as seen in figure 4.1. When measuring the MIS capacitor the admittance is measured. The admittance is defined as $Y = G_m + j\omega C_m$ where G_m is the measured conductance, C_m is the measured capacitance, ω is the angular frequency and j is the complex number $\sqrt{-1}$.

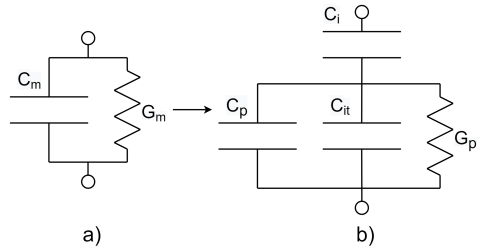

Figure 4.1: a) Simple circuit diagram of the measured MIS capacitor. b) Equivalent circuit of the MIS capacitor. G_m is the measured conductance, C_m is the measured capacitance, C_{it} is capacitance due to interface traps, C_i is the insulator capacitance, C_p and G_p are the parallel capacitance and conductance respectively.

Band diagram of an n-type SiC/insulator interface can be seen in figure 4.2. The figure shows the condition of the energy bands of the SiC and the insulator under different biasing condition. For n-type, accumulation condition means electrons have accumulated at the interface effectively collecting negative charge at the SiC/insulator interface, C_p is a capacitor that theoretically $\rightarrow \infty$ when electrons accumulate at the interface thus

$C_p >> C_{it}$, however, in accumulation the C_i is a fixed capacitor in series thus capping the capacitance in accumulation and the MIS capacitor reaches its maximum capacitance and $C_m = C_i$. Flatband condition means the energy bands of the SiC and the insulator are flat, the net charge on both sides of the insulator is then zero. Depletion condition means electrons are leaving the interface creating a depletion region that extends into the SiC leaving a net positive charge at the SiC/insulator interface. This positive charge is due to the ionized nitrogen donors in the epilayer. In accumulation electrons that are accumulated at the interface will be captured by interface or near interface traps. SiC is a large band gap semiconductor and has therefore a very low thermal generation of minority carriers. In depletion there is no inversion without external influence (for example UV illumination) in the MIS structure.

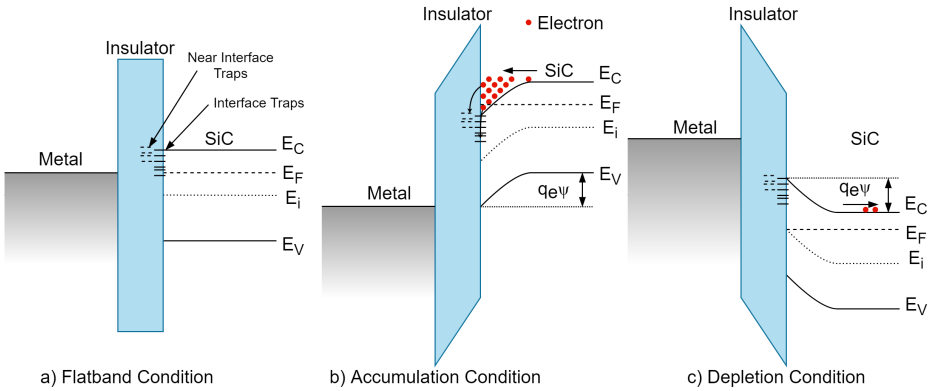

Figure 4.2: Band diagram of an ideal n-type SiC/insulator interface. a) Flatband condition, conduction band and valence bands are straight. b) Accumulation condition, conduction and valence bands are bending upwards accumulating electrons at the interface. c) Depletion condition, conduction and valence bands curve downward depleting the interface of electrons.

In following chapters the theory of semiconductor physics is derived from [62]–[66].

4.1 Capacitance-Voltage Measurements

Capacitance-Voltage (CV) measurements can provide the insulator thickness (t_i), flatband voltage (V_{fb}), net doping concentration (N_D for n-type and N_A for p-type) of the SiC epilayer and the density of interface traps (D_{it}) located at the SiC/insulator interface.

Using capacitance voltage measurements it is possible to extract the

density of interface traps located at or near the SiC/dielectric interface using so called Hi-Lo CV method. For Hi-Lo measurements a direct current (DC) bias is applied to the MIS capacitor coupled with an alternating current (AC) test signal where the AC test signal has different frequencies, we used 1 kHz, 10 kHz, 100 kHz and 1MHz. Therefore, Hi is the higher frequency and Lo is the lower frequency,

The measurements are performed at different fixed temperatures as the thermal electron capture and emission rate from traps at the interface follows

$$e_n = \sigma_c v_{th} N_C exp\left(- \frac{E_C - E_T}{k_B T} \right) \tag{4.1}$$

where σ_c is the capture cross section of the trap, v_{th} is the thermal velocity of the electron in the conduction band, N_C is the effective density of states in the SiC conduction band, $E_C - E_T$ is the activation energy of the trap, k_B is the Boltzmann constant and T is the temperature at which the measurement is performed. Equation 4.1 describes the frequency response of traps located at some energy below the conduction band edge. Applying test signal with different frequency will give different capacitance spectra. This is due to capture rate of interface traps being normally much higher than the emission rate of the trap. If the test frequency is above the emission rate the electron is captured but not re-emitted resulting in a shift in the CV curve to the right. This will show up as a frequency dispersion in the CV spectra as can be seen in figure 4.3. Because of this an energy interval can be found where traps respond to the test signal at a fixed temperature.

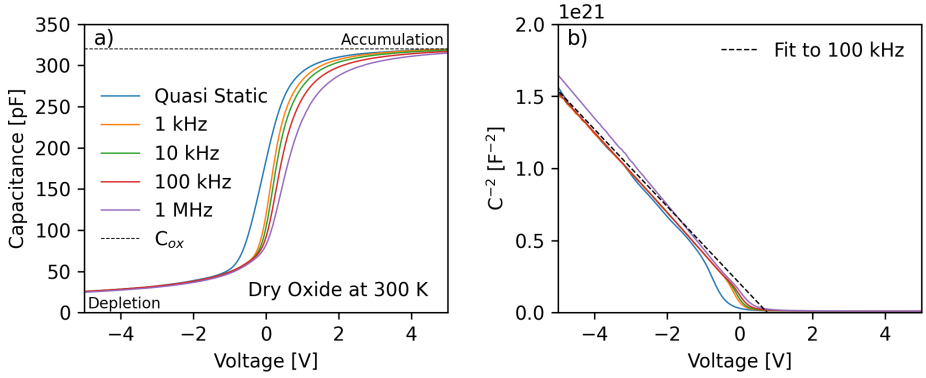

Figure 4.3: a) Capacitance voltage curves of dry oxide at 300 K using quasi static, 1 kHz, 10 kHz, 100 kHz and 1 MHz frequencies. b) $1/C^2$ vs voltage used to extract the slope $d(1/C^2)/dV$ for calculation of the net doping concentration within the epilayer.

Measuring the deep depletion of a MIS structure allows one to extract the doping concentration of the epilayer using the $1/C^2$ vs. voltage graph (see figure 4.3 b)) as it follows the relation

$$N_D = \frac{2}{q_e \epsilon_{SiC} A^2 (\frac{d1/C^2}{dV})} \tag{4.2}$$

where N_D is the epilayer doping, q_e is the elementary charge, ϵ_{SiC} is the dielectric constant of the semiconductor multiplied with the permittivity of vacuum and A is the area of the MIS capacitor.

To extract the insulator thickness (t_i) a high enough voltage is applied to the MIS structure to accumulate the interface. From the CV graph the insulator capacitance (C_i) can be extracted as the max value of the CV curve in high accumulation. Using C_i the thickness of the insulator can be extracted using

$$t_i = \frac{\epsilon_0 \kappa A}{C_i} \tag{4.3}$$

where ϵ_0 is permittivity of vacuum and κ is the dielectric constant of the insulator. The flatband voltage is extracted by first calculating the flatband capacitance using

$$C_{fb} = \frac{\epsilon_i}{t_i + (\epsilon_i/\epsilon_{SiC}) L_D} \tag{4.4}$$

where $\epsilon_i = \kappa\epsilon_0$ is the permittivity of the insulator and L_D is the Debye length given with

$$L_D = \sqrt{\frac{\epsilon_{SiC} k_B T}{q_e^2 N_D}} \tag{4.5}$$

Matching the calculated C_{fb} to the measured capacitance curve allows one to extract the flatband voltage.

The quasi static measurements are done by sweeping the gate voltage of the MIS structure at a constant rate and measuring the charge Q thus the capacitance can be calculated using

$$C_{QS} = \frac{dQ}{dV} \tag{4.6}$$

From the Hi-Lo method the density of interface traps is given by

$$D_{it} = \frac{C_i}{q_e A} \left(\frac{C_{lo}/C_i}{1 - C_{lo}/C_i} - \frac{C_{hi}/C_i}{1 - C_{hi}/C_i} \right) \tag{4.7}$$

where C_{lo} is the capacitance at the lower frequency and C_{hi} is the capacitance at the higher frequency used in the measurements, we used quasi static

capacitance as C_{lo} and 1 MHz capacitance as the C_{hi}. This is done because we assume all traps can follow the quasi-static measurement. While at higher frequencies, traps with too slow response time cannot follow the test signal and thus lead to shift in the CV curve. Using the quasi static capacitance gives more accurate results as it reveals slower traps that cannot follow the 1 kHz test signal. The energy is calculated from the surface potential position as a function of the applied gate voltage to the MIS structure. First the semiconductor capacitance is calculated as a function of the surface potential ψ_s using

$$C_s(\psi_s) = \frac{Aq_eN_D|exp\Big(\frac{q_e\psi_s}{k_BT}\Big) - 1|}{\sqrt{\frac{2k_BTN_D}{\epsilon_{SiC}}\Big\{exp\Big(\frac{q_e\psi_s}{k_BT}\Big) - \frac{q_e\psi_s}{k_BT} - 1\Big\}}} \tag{4.8}$$

then the extracted accumulation capacitance C_i is used to get a theoretical curve of the measured MIS capacitor

$$C_{theory} = \left(\frac{1}{C_s} + \frac{1}{C_i}\right)^{-1} \tag{4.9}$$

The measured 1 MHz curve is then compared to the theoretical capacitance, C_{theory}, to extract the position of the surface potential as a function of the applied voltage to the MIS capacitor as seen in figure 4.4 c).

In intrinsic semiconductors the Fermi level is located close to the middle of the bandgap at room temperature. By doping the semiconductor the Fermi level moves either towards the conduction band if doped with n-type dopant or towards the valence band if doped with p-type dopant. The traps at the SiC/insulator interface respond to the test signal when the Fermi level at the interface is equal to the trap level. The location of the Fermi level at the interface is given by

$$E_C - E_T = E_F - \psi_s \tag{4.10}$$

where E_C is the energy of the conduction band edge, usually chosen as 0 eV because it is the reference point, E_F is the Fermi level location below the SiC conduction band edge given by

$$E_F = \frac{k_BT}{q_e} ln\Big(\frac{N_C}{N_D}\Big) \tag{4.11}$$

where N_C is the effective density of states in the SiC conduction band. Using the Hi-Lo method the density of interface traps can be extracted at different energy intervals that are bound by equation 4.1.

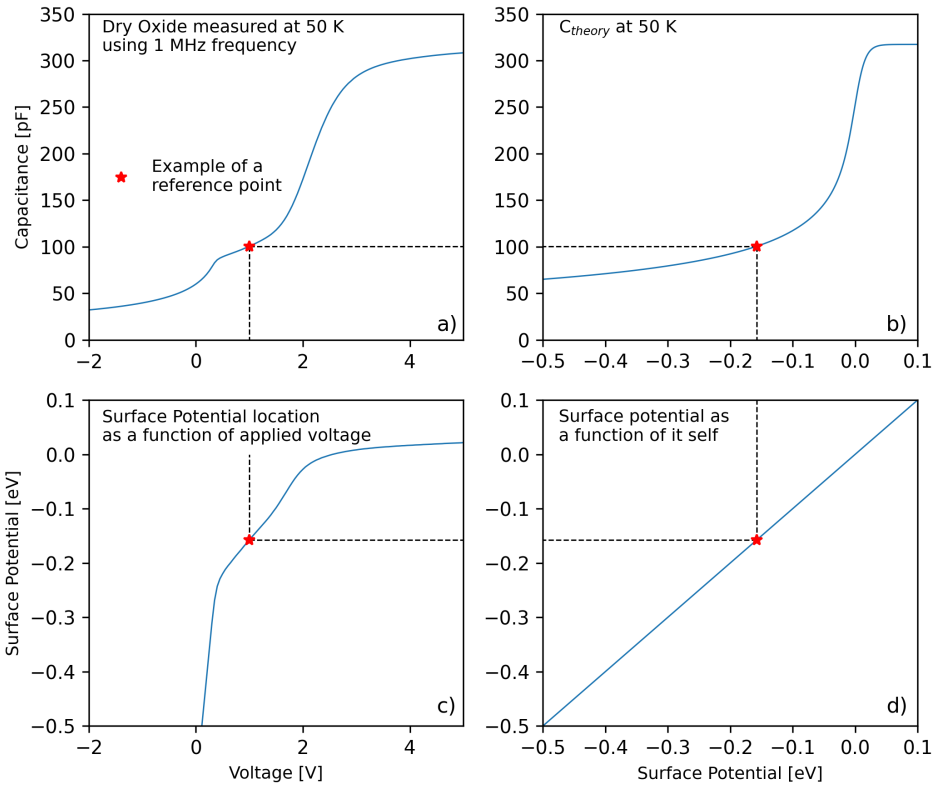

Figure 4.4: a) CV curve of dry oxide MOS capacitor measured at 50 K using 1 MHz test signal. b) Theoretical capacitance of the measured MOS capacitor at 50 K. c) Surface potential as a function of the applied voltage. d) Surface potential as a function of itself.

In figure 4.5 a CV spectra of a dry oxide at different temperatures and the extracted D_{it} at each temperature respectively can be seen. The frequency dispersion that is formed in the CV spectra as the temperature is lowered depends on how traps respond to the AC test signal. When cooling down the traps at fixed energies reduce their capture/emission rate following equation 4.1. Thus traps no longer respond beyond some frequency as electrons are captured but not re-emitted and this gives rise to frequency dispersion.

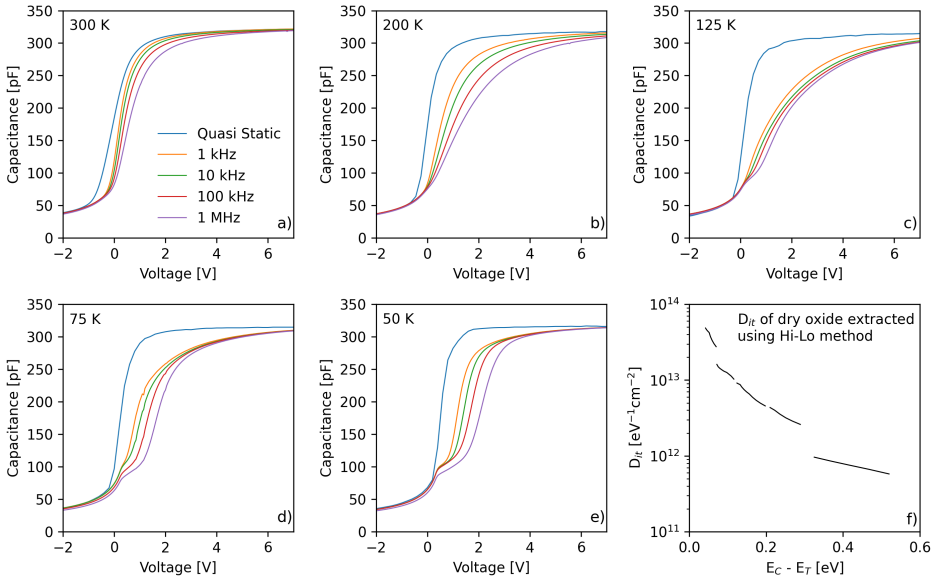

Figure 4.5: a) - e) CV measurements of a dry oxide sample at different temperatures at quasi static, 1 kHz, 10 kHz, 100 kHz and 1 MHz. f) Density of interface traps extracted at each temperature.

4.2 Conductance Spectroscopy Measurements

4.2.1 Conductance as a Function of Temperature

Conductance spectroscopy can be performed in many different ways, the most common one is to measure the conductance as a function of test frequency at a fixed voltage and temperature. Other method is to cool down to cryogenic temperatures and at low temperatures apply a fixed bias and ramp up the temperature at a fixed rate while monitoring the conductance as function of temperature. Both methods have their usefulness and follow the same physical principles to extract physical parameters of traps located within the SiC bandgap. These methods are usually performed using low frequencies, 1 MHz and under, due to series resistance that gets more effective at higher frequencies and inductance in the setup cabling.

The measurements are done in weak depletion thus the parallel conductance can be extracted from the measured data using

$$\frac{\langle G_p \rangle}{\omega} = \frac{\omega C_i^2 G_m}{G_m^2 + \omega^2 (C_i - C_m)^2} \tag{4.12}$$

where C_i is the accumulation capacitance of the MIS capacitor. The D_{it} is connected to the peak amplitude in the conductance spectra with [62]

$$\left(\frac{\langle G_p\rangle}{\omega}\right)_{f_{peak}} = \frac{q_e^2 A D_{it}}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{+\infty} \frac{ln(1+(\omega\tau exp(\eta))^2)}{2\omega\tau exp(\eta)} \times exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) d\eta \quad (4.13)$$

where σ_s is the standard deviation of the peak width that appears in the conductance vs. frequency spectra, τ is the time constant of the interface traps and η is $v_s - \langle v_s\rangle$, where v_s is the band bending and $\langle v_s\rangle$ is the mean of the band bending. The capture cross section (σ_c) and the energy location of the traps are connected to the temperature location of the peak and the frequency of the $\langle (G_p/\omega)_{f_{peak}}\rangle$ by

$$\sigma_c = \frac{1}{\tau_{peak} v_{th} N_C} exp\left(\frac{E_C - E_T}{k_B T_{peak}}\right) \quad (4.14)$$

where

$$\tau_{peak} = \frac{\alpha(\sigma_s)}{2\pi f_{peak}} \quad (4.15)$$

where $\alpha(\sigma_s)$ is a factor extracted from the standard deviation of the conductance peak and was found to be 2.5. Measuring the temperature and frequency dependency of the conductance, the $E_C - E_T$ and σ_c can be determined by using Arrhenius analysis while assuming $v_{th}N_C$ is proportional to the square of the peak temperature and that σ_c is independent of temperature.

Figure 4.6 shows a conductance vs. temperature spectra of a dry oxide between 50 and 300 K. The peaks noted as $N(c)$, NI and OX are the dopant peak related to nitrogen (N) doping atoms located in cubic sites in the 4H-SiC epilayer, very fast interface traps and slow interface traps respectively.

Figure 4.7 shows the same conductance spectra of a dry oxide as figure 4.6 where the individual peaks are zoomed into and the relationship between $\tau_{peak}T_{peak}^2$ and T_{peak}^{-1}.

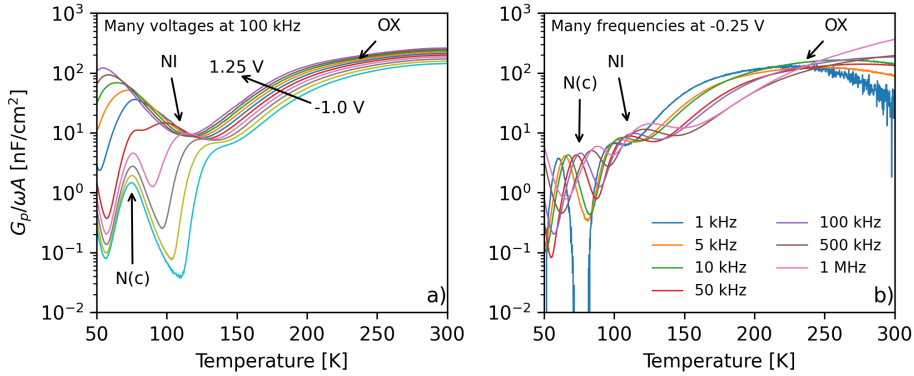

Figure 4.6: a) Conductance spectra of dry oxide at many voltages, voltage step is 250 mV between measurements. b) Conductance spectra of dry oxide at all test frequencies at -0.25 V. Test frequencies are 1 kHz, 5 kHz, 10 kHz, 50 kHz, 100 kHz, 500 kHz and 1 MHz.

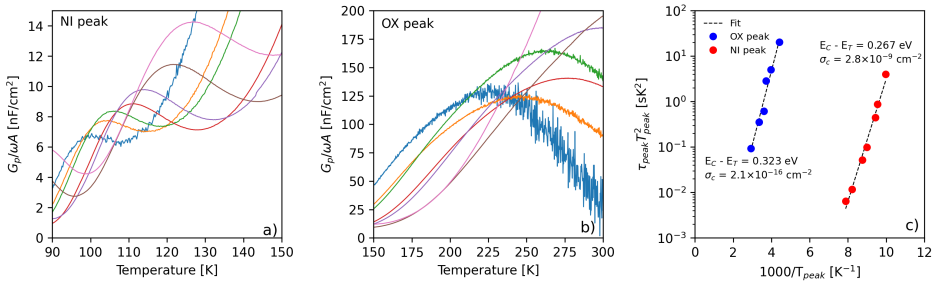

Figure 4.7: a) Conductance spectra of a dry oxide at different frequencies where zoomed into the NI peak. b) Conductance spectra of a dry oxide where zoomed into the OX peak. c) Relationship between $\tau_{peak}T^2_{peak}$ and T^{-1}_{peak}, and relevant results of $E_C - E_T$ and σ_c.

4.2.2 Conductance as a Function of Frequency

Traditionally conductance spectroscopy is made at a fixed temperature and voltage while the frequencies are changed. The advantage of this method is that the probed peak is much clearer and important parameters can be extracted such as the standard deviation $\alpha(\sigma_s)$, $E_C - E_T$ and capture cross section σ_c. However, measurements need to be done at many temperatures to get a clear picture and statistically significant results. Figure 4.8 shows conductance as a function of angular frequency ω spectra at several temperatures and the extracted energy and capture cross section.

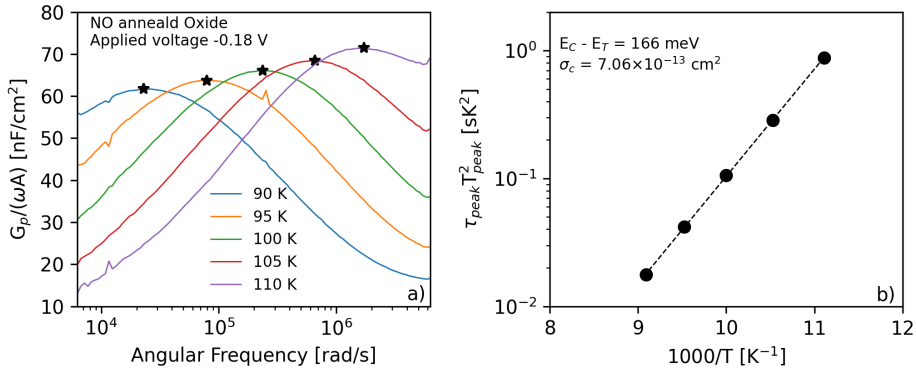

Figure 4.8: a) Conductance as function of angular frequency of NO annealed SiO_2 oxide at 90, 95, 100, 105 and 110 K with peak values highlighted. b) Relationship between $\tau_{peak}T^2_{peak}$ and T^{-1}_{peak} and relevant results of $E_C - E_T$ and σ_c.

4.2.3 Conductance of a Schottky Diode

Schottky diode structure is a simpler structure than the MIS structure since there is no insulator between the metal contact and the semiconductor. The Schottky diode can be used to probe bulk defects in the semiconductor and thus is useful to determine the physical locations of defects if they are detected both in MIS and Schottky structures. Conductance measurements on a Schottky diode can be performed in similar fashion to that of a MIS structure. However, extracting the parallel conductance is a little different from that of equation 4.12 because now there is no insulator thus no C_i. The parallel conductance of Schottky diode is given by [64]

$$\frac{G_p}{\omega} = \frac{G_m(1 + r_s G_m) + r_s(\omega C_m)^2}{(1 + r_s G_m)^2 + (\omega r_s C_m)^2} \cdot \omega^{-1} \tag{4.16}$$

where r_s is the series resistance of the Schottky diode and can be extracted by forward biasing the Schottky until it hits the linear region of the current vs voltage spectra where the series resistance is limiting the current.

4.3 Thermal Dielectric Relaxation Current Measurements

The thermal dielectric relaxation current (TDRC) can be applied in many different ways [67]. Details of the TDRC theory can be found in papers by J. G. Simmons, H. A. Mar and L. S. Wei [68]–[70]. TDRC is a two

stage method. First an accumulative bias is applied at room temperature (sometimes it is better to cool to 250 K before applying the bias if the sample has mobile sodium ions at the interface, this makes the ions less mobile), then the MIS capacitor sample is cooled down to cryogenic temperatures with applied accumulation bias. This will trap electrons in defects at the interface. At cryogenic temperature the bias is switched to depletion and the sample is heated up to room temperature at a fixed ramp rate, we used 5 K/min, while the current is monitored. When the sample is heated the electrons that were trapped in interface defects are thermally emitted and a current can be detected. The area $\mathcal{A}$ under the TDRC signal curve is defined by

$$\mathcal{A} = \int_{T_0}^{T_1} (-J(T))dT = q_e \beta N_{it} \tag{4.17}$$

where T_0 and T_1 are the start and stop temperatures respectively, J is the current density, β is the ramp rate and N_{it} is the number of traps at the interface that produce the TDRC current. The electric field across the insulator during charging is $E = (V - V_{fb})/t_i$ where V is the applied accumulative voltage. Figure 4.9 shows the current density signal of a dry oxide and the extracted number of traps at the interface as a function of the accumulation electric field while cooling. The two peaks in the TDRC signal

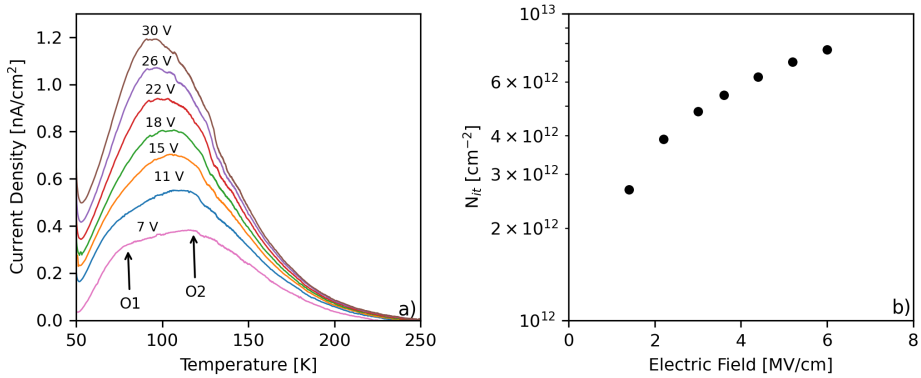

Figure 4.9: a) TDRC measurements of dry oxide at several different accumulative voltage and same discharge depletion voltage. b) Number of traps extracted from the TDRC signal at each electric field.

noted as O_1 and O_2 are slow traps with energy levels inside the SiC energy band gap. O_1 has been found to have activation energy of 110 meV while O_2 has wide activation energy distribution from 100 - 800 meV [67], [71], [72].

4.4 Subthreshold Swing and Electron Mobility in MISFETs

The switching speed of a MISFET is determined by how fast the MISFET can be turned on and off, meaning how fast can the MISFET channel be charged and discharged with the applied gate voltage. The subthreshold swing is measured as change in voltage over one decade of current in the channel between drain and the source called I_{ds}. The subthreshold swing is defined by [73]

$$SS \equiv ln(10)\frac{dV_G}{d(ln(I_{DS}))} \tag{4.18}$$

where V_G is the applied gate voltage and I_{DS} is the current between the drain and the source. Equation 4.18 can also be written as

$$SS \simeq ln(10)\frac{k_B T}{q_e}\left(1 + \frac{C_d}{C_i}\right) \tag{4.19}$$

where C_d is the depletion capacitance. The subthreshold swing is theoretically limited by the $ln(10)k_BT/q_e$ known as the thermionic limit where we let $C_d \to 0$ and/or $C_i \to \infty$ giving the limit of $S \approx 60\ mV/dec$ at 300 K.

The mobility of the MISFET is highly determined on the quality of the SiC/insulator interface as well as few other factors. The field-effect mobility of electrons moving across the MISFETs channel from source to the drain is given by

$$\mu_{FE} = \frac{Lg_m^i}{WC_iV_{DS}} \tag{4.20}$$

where L and W are the length and width of the gate respectively, V_{DS} is a constant voltage potential between drain and source (V_{DS} has to be low to ensure the MISFET is within the linear region, we used 0.1 V), and g_m^i is the MISFETs transconductance defined as $g_m^i = \partial I_{DS}/\partial V_G$ thus equation 4.20 becomes

$$\mu_{FE} = \frac{L}{WC_iV_{DS}} \cdot \frac{\partial I_{DS}}{\partial V_G} \tag{4.21}$$

Figure 4.10 shows drain-source current (I_{DS}) and mobility as function of applied gate voltage with the subthreshold slope and peak mobility marked.

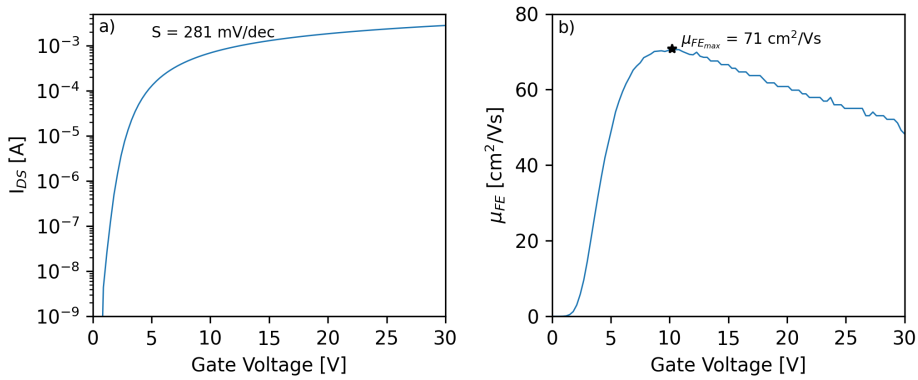

Figure 4.10: MOSFET with SiO_2 gate oxide that has been grown using the SEO method. a) I_{DS} vs V_G curves with subthreshold slope results. b) Field-effect mobility as a function of the applied gate voltage with the peak mobility marked.

4.5 Scanning Transmission Electron Microscopy and Electron Energy Loss Spectroscopy

Scanning transmission electron microscopy in combination with electron energy loss spectroscopy was performed on the AlN and Al_2O_3 samples to investigate the SiC/AlN and SiC/Al_2O_3 interfaces. The two samples are prepared using mechanical cutting, mechanical polishing and Ar-ion thinning (Gatan PIPS Model 691) at a 5° angle. The imaging and spectroscopy were performed at 300 keV on the Linköping double-corrected FEI Titan^3 60-300. Images were acquired in high-angle annular dark-field (HAADF) mode with collection semi-angles between ∼60 and 200 mrad. Series of images were reconstructed using *Smart-Align* [74] for Digital Micrograph (Gatan Inc.). The EELS was performed using a GIF Quantum ERS detector (Gatan Inc.), with a convergence semi-angle of 22.0 mrad and a collection semi-angle of 56.5 mrad. It was operated in dual-EELS mode with dispersions of 0.05 in the ranges of -10.0 – 92.4 and 50.0 – 152.4 eV, for Al and Si $L_{2,3}$-edges, or 490.0 – 592.4 eV, for C and O K-edges. Additionally, 0.25 eV/channel was used in the ranges of -50.0–462.0 and 50.0–562.0 eV, for the all the edges mentioned above as well as the N K-edge. The scans were acquired as spectrum images of sites neighbouring the sites where high-resolution images were acquired. Subsequently these were integrated along the interface to form linescans with spectra in each pixel. The intensity of each element as a function of position was calculated by removal of background according to a power law and the signal intensity integrated from the onset energy

and ∼50 eV above. Unfortunately, background subtraction is not enough to distinguish Si from Al, as they are overlapping. The Si intensity presented is hence calculated by subtracting the Al intensity from the measured intensity at the Si onset: $I_{Si,real} = I_{Si} - I_{Al}$, where $I_{Si,real}$ denotes the real Si-intensity, I_{Si} the measured intensity at Si onset energy, and I_{Al} the measured intensity at Al onset energy.

4.6 Samples Preparation and Parameters

All MIS samples used in this study are made using 4H-SiC substrates with 4° off axis cut. Table 4.1 lists samples used in this study, their fabrication methods and thicknesses. In this study, few dry oxide samples where used as reference samples. They were made in different furnaces which explains the different oxide thicknesses even if they were made using similar oxidation times and temperature. The 4 times thicker SEO sample can be explained by the enhanced oxidation rate in the presence of sodium while the oxide is grown [34]. SEO samples can have a difference in thickness of up to 10 nm from one edge of a samples piece to the other edge. Furthermore placing the Al_2O_3 carrier boats that provide the sodium contamination, at different positions in the furnace will cause different oxidation rates.

In chapter 5 we use dry oxide sample # 2 and SEO sample # 2 from table 4.1 to discuss the measurements results.

MIS-Capacitors	Processing Method	Dielectric Thickness
Dry SiO_2 #1	Dry oxidation at 1250°C for 60 minutes	50 nm
Dry SiO_2 #2	Dry oxidation at 1250°C for 60 minutes	44 nm
Dry SiO_2 #3	Dry oxidation at 1240°C for 40 minutes	32 nm
N_2O	Grown in N_2O ambient at 1240°C for 180 minutes	50 nm
NO	Dry oxidation at 1250°C for 60 minutes with post anneal in pure NO at 1250°C for 60 minutes	41 nm
SEO #1	Thermally oxidized at 1200°C for 40 minutes in Al_2O_3 carrier boats that are Na contaminated	192 nm
SEO #2	Thermally oxidized at 1200°C for 40 minutes in Al_2O_3 carrier boats that are Na contaminated	52 nm
Al_2O_3	Depositing 1-2 nm layer of Al with e-beam evaporation at 0.5 Å/s deposition rate, the samples are taken out and baked at 200°C on a hot plate for 5 minutes, repeated 12 times	15 nm
AlN	Metal-Organic Chemical Vapor Deposition (MOCDV) at 1100°C [55]	30 nm
SiC/Al Diode	Aluminium deposited on the SiC epilayer using e-beam evaporation after HF etching	
MOSFETs	Processing Method	Dielectric Thickness
Dry SiO_2	Dry oxidation at 1100°C for 120 min	60 nm
N_2O	Grown in N_2O ambient at 1240°C for 180 minutes	55 nm
SEO #1	Thermally oxidized at 1200°C for 40 minutes in Al_2O_3 carrier boats that are Na contaminated	188 nm
SEO #2	Thermally oxidized at 1200°C for 40 minutes in Al_2O_3 carrier boats that are Na contaminated	100 nm

Table 4.1: Table listing fabrication methods of samples used in this study.

Chapter 5

Results of Electrical Analysis

5.1 Conductance Spectroscopy

5.1.1 Conductance of MIS Capacitors

Conductance spectroscopy is done by cooling to 50 K without bias applied to the MIS structure, and then at 50 K a bias is applied and the sample is heated to 300 K with fixed ramp of 5 K/min while the conductance and capacitance are monitored. Figure 5.1 shows the conductance spectroscopy of all samples using 100 kHz and 10 mV AC test signal. The measurements are repeated several times with gate bias corresponding to the weak depletion region.

Figure 5.1 a) shows the dry oxide. The peak marked at about 75 K is due to the nitrogen dopant ions located at cubic sites, the rising signal above 250 K, noted as OX, is due to the slow oxide traps that have energy levels within the SiC energy bandgap with activation energy of about 0.35 eV. The peak that appears first at about 175 K as a small hump in the larger OX signal, noted as NI, and moves to lower temperatures when higher bias is applied to the MOS capacitor is due to very fast interface traps.

Figure 5.1 b) shows the N_2O grown sample. The N_2O grown sample has reduced signal from the OX traps indicating passivation of the slow traps. However the NI signal is now very clear and is slightly larger than in the dry oxide sample suggesting that the N_2O treatment is promoting the NI trap.

Figure 5.1 c) shows the NO annealed sample. The OX signal has been suppressed like in the N_2O grown sample but the NI signal is even larger than before.

Figure 5.1 d) shows the SEO sample. The OX signal is suppressed significantly and there is no NI peak that appears with higher applied bias. The small peak at about 140 K is a signal within the depletion layer and is probably from titanium (Ti) acceptor impurities in the SiC epilayer having activation energies around 150 - 170 meV [75]. It is evident that the NI trap is absent or below the detection limit in the SEO sample.

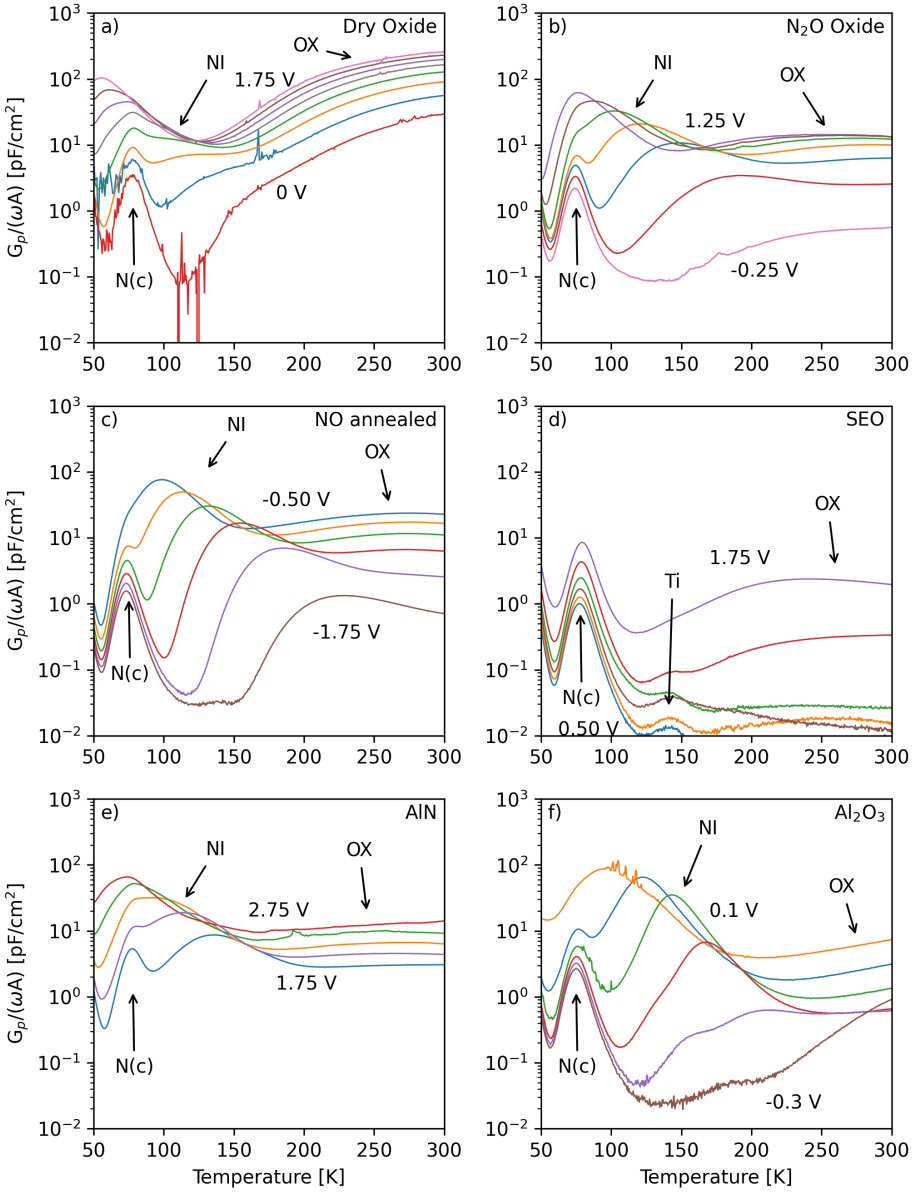

Figure 5.1: Conductance spectroscopy of all samples from 50 K to 300 K using 100 kHz 10 mV AC test signal at differently applied weak depletion bias. a) Dry oxide, b) N_2O grown oxide, c) NO annealed oxide, d) SEO oxide, e) AlN gate dielectric and f) Al_2O_3 gate dielectric.

Figure 5.1 e) shows the AlN sample. The OX signal is low and flat but the NI peak signal does show up at about 175 K and shows the same behaviour as in the SiO_2 samples in figures 5.1 a) - c). This suggests that the NI signal is not inherently related to the SiO_2 but rather to the SiC epilayer.

Figure 5.1 f) shows the Al_2O_3 sample. Similar to the AlN the Al_2O_3 shows low OX signal but the NI peak does appear at higher applied voltages and shows the same behaviour as in other samples.

The fact that the NI signal is observed in both the AlN and Al_2O_3 samples where the interfaces are smooth and not oxidized from the growth of the dielectrics suggests that the physical origin of the NI signal is probably not a property of the dielectric but rather a property of the SiC surface. Though the cause of the NI signal is still unknown it appears that the NI trap is not related to the oxidation of the SiC/SiO_2 interface as has been suggested before in publications.

Arrhenius analysis can be applied to the NI signal to extract its energy, D_{it} and capture cross section, σ_c, and the results are shown in figure 5.2. It shows how the extracted values of energy and the capture cross section have a very wide distribution from about 60 meV to 350 meV in energy and about 10^{-11} - 10^{-16} cm^2 for the capture cross section. Previous studies have reported up to 10^{-9} cm^2 [13]. This is unusual for traps located directly at the SiC/dielectric interface. Capture cross section larger than about 10^{-13} cm^2 are not physically realistic for a trap which suggests that the assumption of NI being conventional interface trap is highly questionable. This data is in good agreement with literature [13]. For the OX traps the peak is

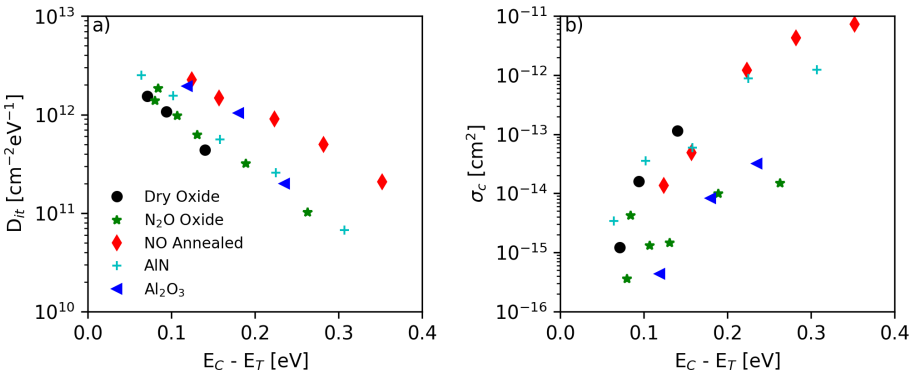

Figure 5.2: Extracted D_{it} and σ_c as function of energy of the NI signal from the conductance spectroscopy using Arrhenius analysis.

relatively localised in temperature in the conductance spectra resulting in

more defined energy interval and σ extracted using the Arrhenius analysis, resulting in energy of 0.27 - 0.4 eV and σ_c of 2.4×10^{-15} - 3.5×10^{-17} cm^2.

5.1.2 Conductance of a Schottky Diode

Considering that the NI signal is visible in samples not containing SiO_2 dielectric suggests that the NI trap is located at the SiC side of the MIS structure. Thus we attempted to measure conductance spectroscopy on a n-SiC/Aluminium diode. The conductance spectra of the SiC/Al diode is shown in figure 5.3. The same nitrogen peak at about 75 K is observed as we observe in the other MIS capacitors samples and the assigned Ti peak is observed as in the SEO sample. However, the NI peak is not observed. The reason why the NI peak is not observed is fairly simple. The NI signal only appears in MIS capacitors when sufficient number of electrons accumulate at the SiC/dielectric interface under weak depletion condition. However, the SiC Schottky diode starts to conduct before sufficient number of electrons can accumulate at the SiC/Al barrier. The SiC/Al barrier is simply to small. Using other metals would not help as the band offset is always too small to enable detection of NI in such a diode.

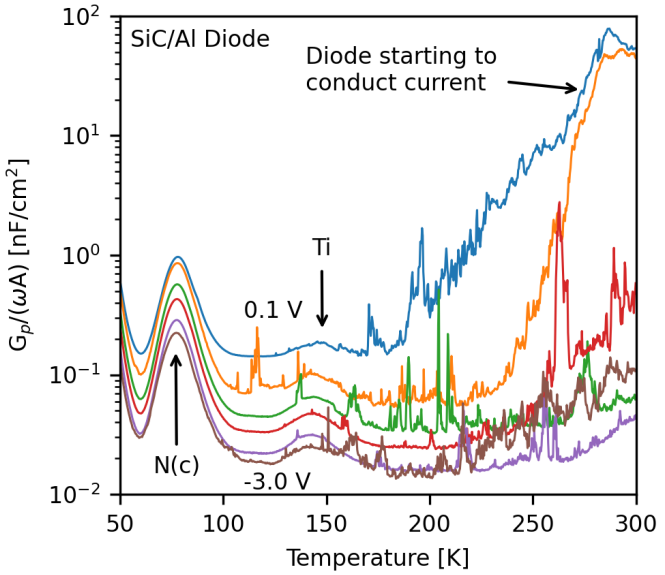

Figure 5.3: Conductance spectroscopy of SiC/Al diode using 100 kHz 10 mV AC test signal from 50 K to 300 K.

5.2 Capacitance Voltage

Capacitance measurements are done at different fixed temperatures from room temperature to 50 K. The MIS capacitors are biased and swept the gate bias from depletion to accumulation using quasi-static and high frequencies. The capacitance spectra of a dry oxide reference sample, N_2O grown, NO annealed, SEO oxide, AlN and Al_2O_3 at 300, 200, 125, 75 and 50 K are shown in figures 5.4 to 5.8. Figure 5.4 a) shows the dry oxide sample at 300 K. The spectra shows significant frequency dispersion compared to all the other samples. The N_2O grown, fig 5.4 b), shows some frequency dispersion, while the NO anneal, SEO, AlN and Al_2O_3 samples show much smaller frequency dispersion. The quasi static curves show a tiny hump or larger frequency dispersion in weak depletion in all samples. The quasi static curve of the Al_2O_3 sample should be interpreted with caution since the curve does not fit well to the higher frequency measurements in depletion, though it shows the same hump in weak depletion that can be seen in the higher frequencies at a similar voltage. The instability of the quasi static curve can be explained by sensitivity of the Al_2O_3 to charge injection and we are using charge voltage measurements to measure the quasi static curve. The frequency dispersion observed at room temperature is due to slow interface traps that correspond to the OX traps in the conductance spectra detailed in chapter 5.1. The label OX refers here to energy distribution of relatively slow interface traps that together give rise to the observed frequency dispersion.

Figure 5.5 shows the capacitance spectra of all samples at 200 K. The frequency dispersion in the dry oxide sample has increased from what is observed at 300 K. Similarly the dispersion has increased in the N_2O grown sample while the NO annealed and the SEO still show a tiny frequency dispersion. The AlN and Al_2O_3 samples show no increase in frequency dispersion. However, the hump that appeared in weak depletion in the Al_2O_3 sample at 300 K has moved to the inflection point where the capacitance starts to rise rapidly. The frequency dispersion at 200 K is assigned to OX traps as the case at 300 K.

Figure 5.6 shows capacitance data of all samples at 125 K. The dry oxide now shows significant stretch out in both accumulation and weak depletion. This would result in an underestimation of the density of interface traps if one would only use 1 kHz and 1 MHz for the D_{it} calculation. When the sample is cooled the emission rate of OX type interface traps decreases and a larger portion of electrons remain trapped and are not able to follow the 1 kHz test signal. However, they are able to follow the signal in the quasi-static measurement and do therefore not affect the quasi-static CV curve. The frequency dispersion in the N_2O sample has increased even more compared

to the 200 K and shows some evidence of stretch out in the accumulation region. The NO annealed sample now shows large frequency dispersion. The SEO sample shows slightly larger dispersion between the quasi static and higher frequencies but for the higher frequencies there is an insignificant dispersion between them indicating that traps giving rise to the frequency dispersion in the NO sample are not present in the SEO sample. The traps responsible for the frequency dispersion in the NO sample are evidently much faster than the OX traps. Furthermore, the onset of the dispersion corresponds to weak depletion and is within the same voltage range as when the NI signal appears in the conductance analysis [76]. We therefore assign the frequency dispersion at 125 K in the NO sample to NI as indicated in figure 5.5 c). The AlN has now started to show some frequency dispersion that was not observed at higher temperatures. The Al_2O_3 sample has now a large frequency dispersion in weak depletion indicating that faster traps closer to the conduction band edge are starting the respond to the test signal.

Figure 5.7 shows the capacitance of all samples at 75 K. The dry oxide still shows evidence of stretch out in accumulation. Additionally a knee has formed in the curve in weak depletion. Similar knee can be observed in the N_2O grown sample and the NO annealed sample. The AlN sample now shows a significant frequency dispersion and the Al_2O_3 has frequency dispersion through out the capacitance spectra. The SEO shows evidence of large series resistance in accumulation in the 1 MHz curve where it accumulates at lower capacitance than the quasi static and the other higher frequencies. Furthermore all samples show frequency dispersion in weak depletion due to the nitrogen doping ions freezing out noted as $N(c)$ in figure 5.7.

Figure 5.8 shows the capacitance spectra of all samples at 50 K. The frequency dispersion has increased even more in the dry oxide, N_2O and NO annealed samples. The knee in the dry, N_2O and NO annealed samples has become even more pronounced and is even bigger in the N_2O and NO annealed samples than the dry oxide samples. The SEO now shows evidence of very large series resistance causing the 10 kHz, 100 kHz and 1 MHz curves not the reach accumulation. This data is thus not useful for extracting the density of interface traps unless using only quasi static and 1 kHz curve but that would underestimate the D_{it}. The AlN show increased frequency dispersion and a small knee, like in the dry, N_2O and NO samples is starting to be noticeable. The Al_2O_3 sample also shows increased frequency dispersion.

The quasi static curve in Al_2O_3 CV spectra shows poor fitting to the higher frequency measurements at all temperatures. This is due to the Al_2O_3 being extremely sensitive to charge injection and leakage and that will have

greater effect at lower frequency measurements.

In summary it is possible to divide the interface traps giving rise to frequency dispersion into two main categories, OX and NI traps. The OX traps are slow traps that are responsible for the frequency dispersion at 300 K and 200 K. At 125 K the dispersion in due to both OX and NI traps. Most of the OX traps are then not able to follow the 1 kHz test signal but do follow the quasi-static measurement and are therefore detected as the difference between the quasi static and 1 kHz curves. The NI trap is faster and is detected as a frequency dispersion between the 1 kHz and 1 MHz curves. At 50 K and 75 K the frequency dispersion between the quasi static and 1 MHz curves is mainly due to the NI trap while the OX traps are providing a significant contribution in the dry oxide. Overall, this interpretation is in line with conductance analysis results presented in chapter 5.1.

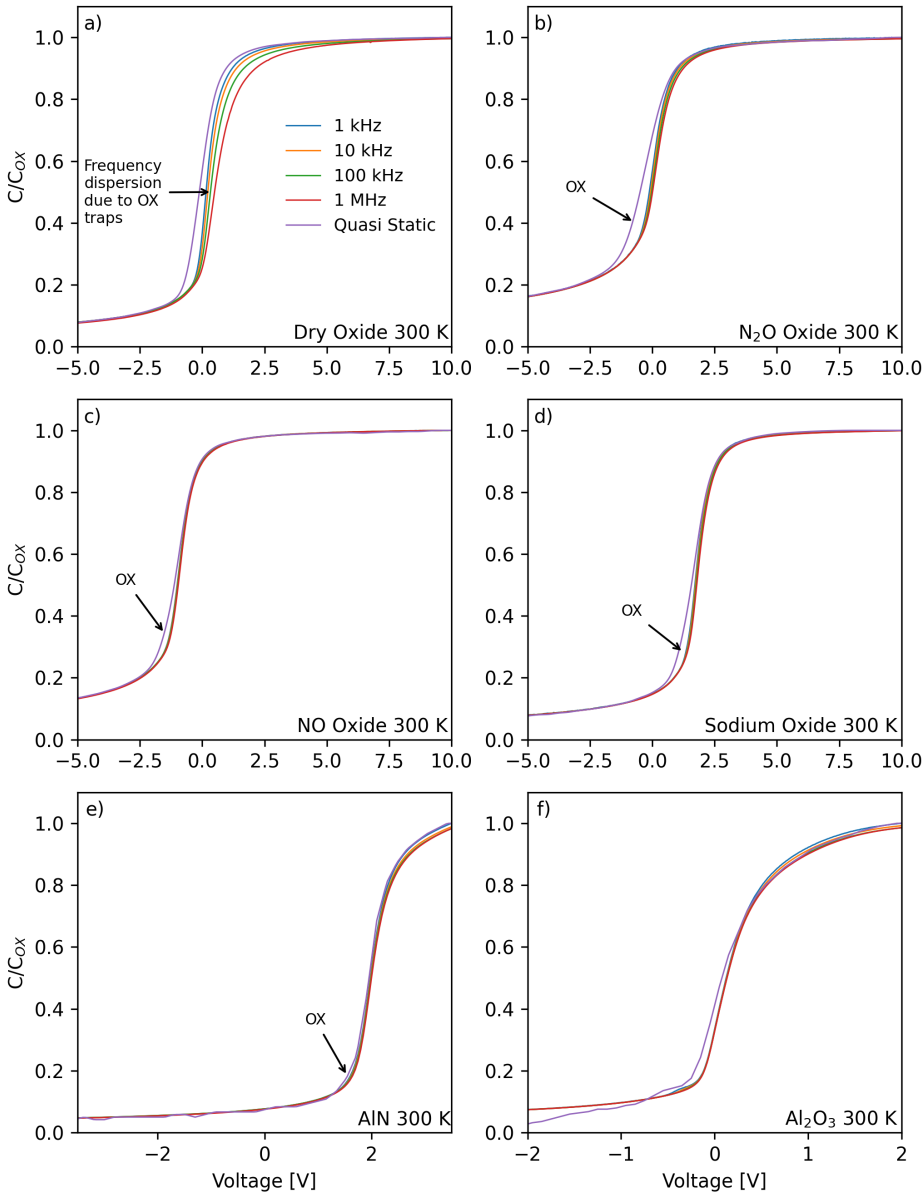

Figure 5.4: Capacitance spectra of all samples at 300 K.

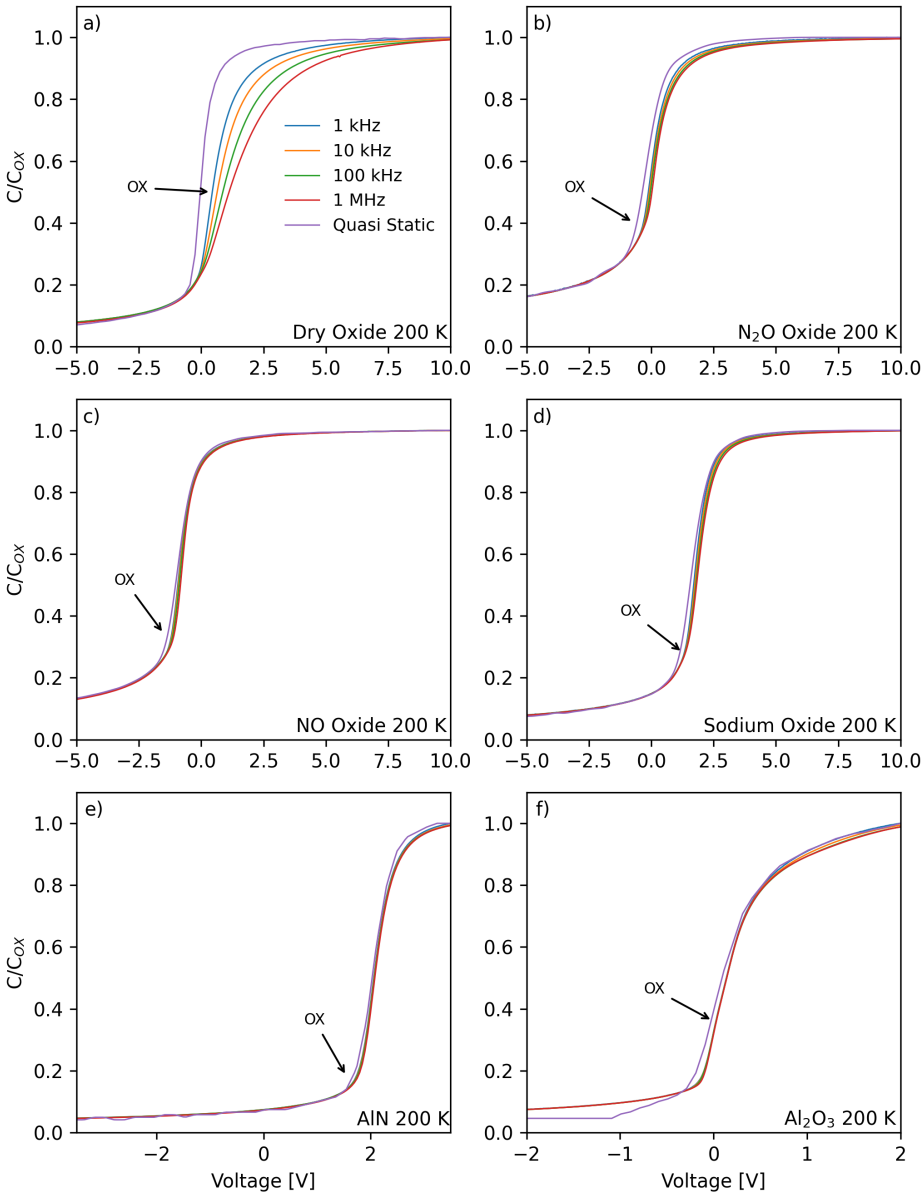

Figure 5.5: Capacitance spectra of all samples at 200 K.

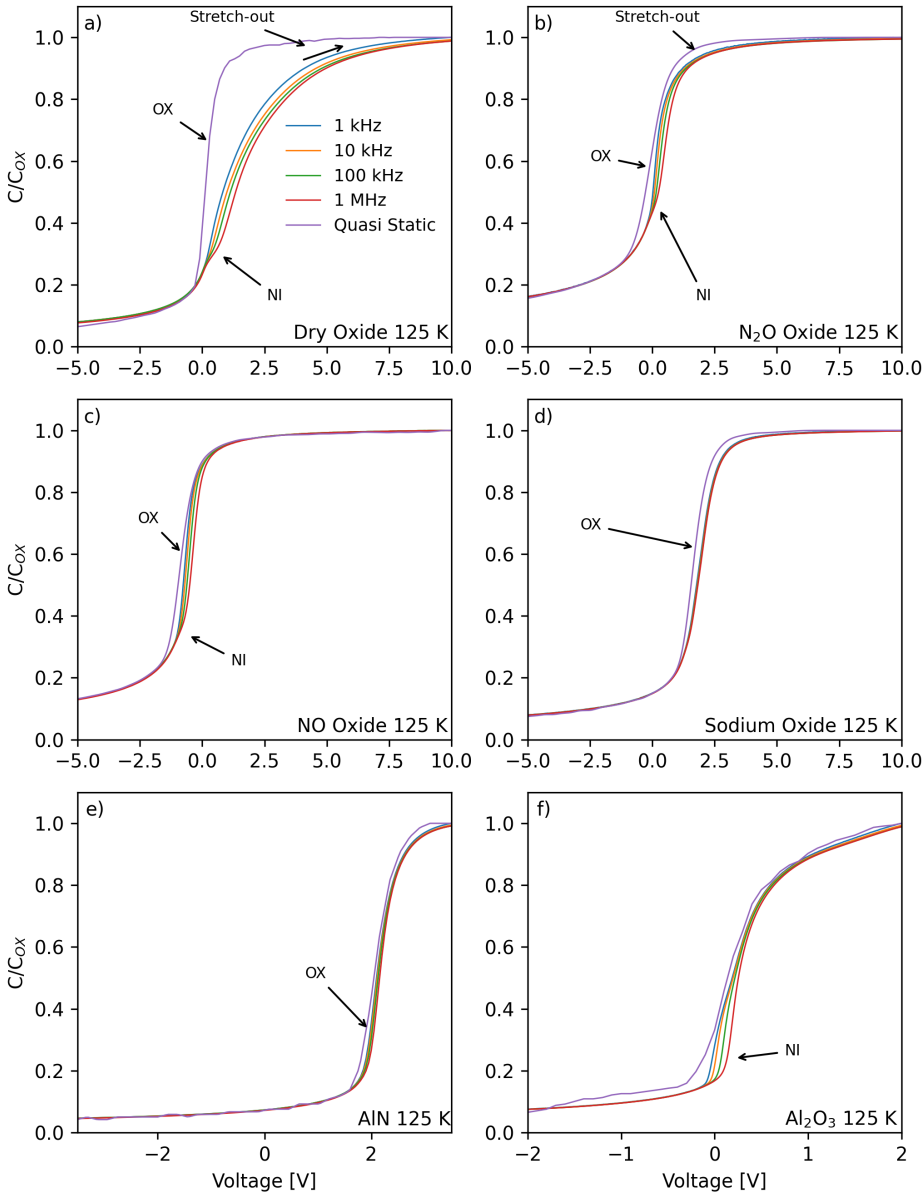

Figure 5.6: Capacitance spectra of all samples at 125 K.

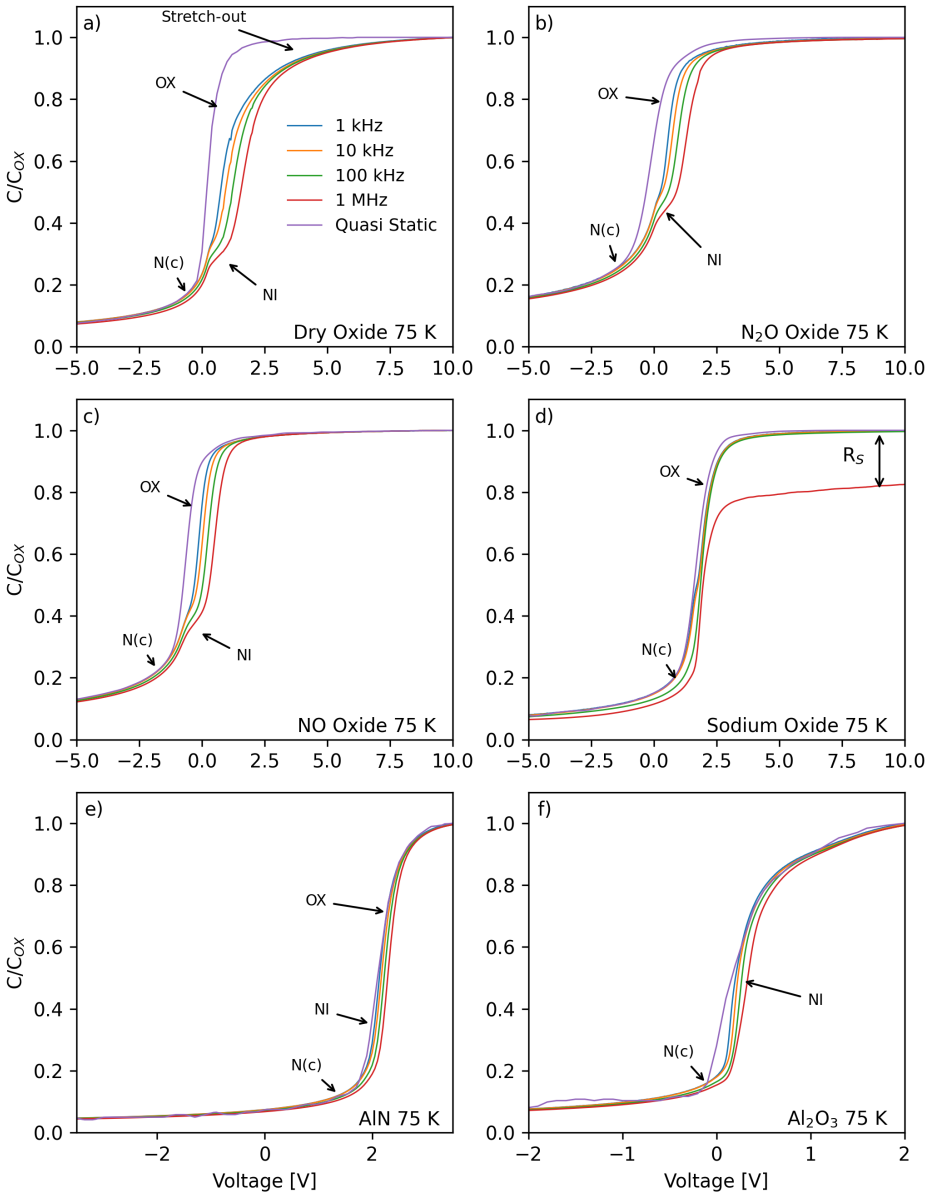

Figure 5.7: Capacitance spectra of all samples at 75 K.

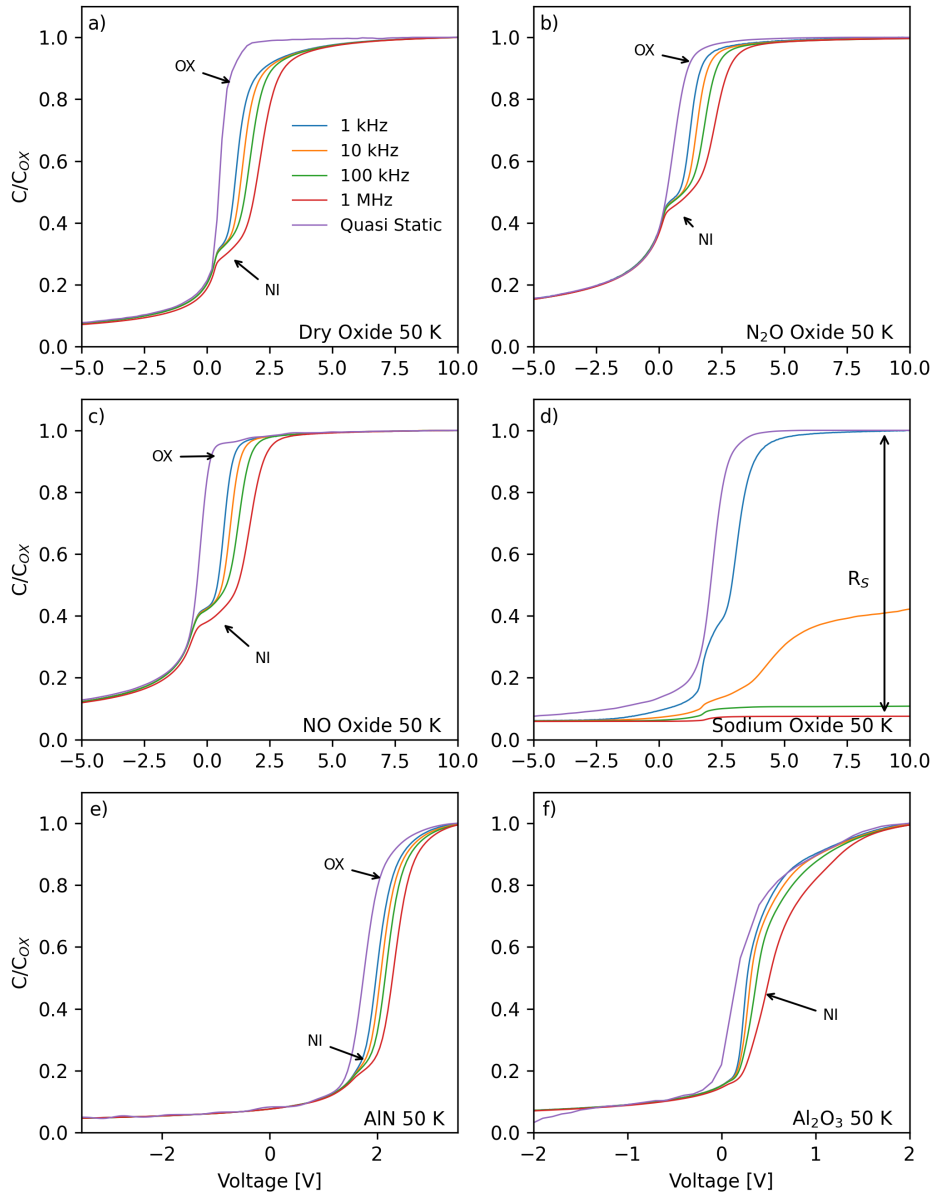

Figure 5.8: Capacitance spectra of all samples at 50 K.

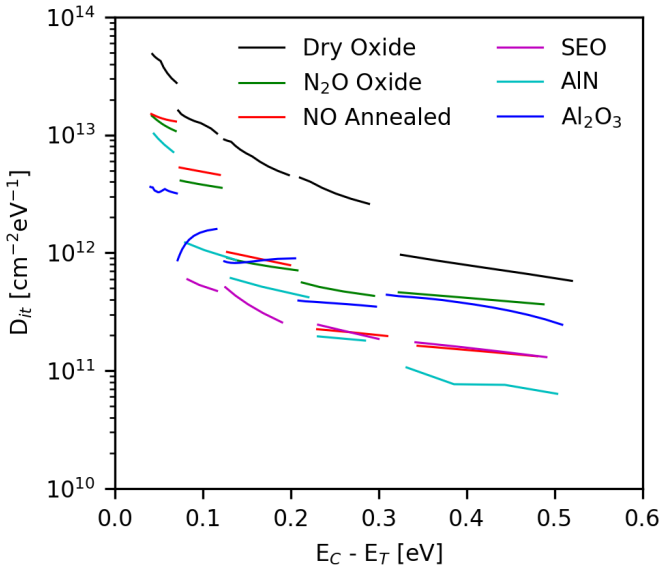

Figure 5.9: Extracted density of interface traps of all samples using quasi static and 1 MHz curves at all temperatures as a function of energy below the SiC conduction band edge.

The extracted D_{it} using quasi static and 1 MHz curves from figure 5.4 to figure 5.8 is shown in figure 5.9. We excluded the extraction of D_{it} from the SEO at 50 K due to the aforementioned high series resistance that prevents accurate analysis of the D_{it}. The dry oxide sample shows the highest density of all samples throughout the energy spectra. At room temperature the D_{it} is roughly around 7.5×10^{11} cm^2eV^{-1} at room temperature or 0.4 eV and increases as we probe closer to the conduction band edge to 4×10^{13} cm^2eV^{-1} at 50 K or 50 meV. The N_2O grown sample shows lower D_{it} than the dry oxide sample throughout the energy spectra but also increases as we probe closer to the conduction band edge from 4×10^{11} cm^2eV^{-1} at 0.4 eV to 1.3×10^{13} cm^2eV^{-1} at 50 meV. The NO sample shows even lower D_{it} than the dry oxide and N_2O grown samples at 0.4 eV of about 1.5×10^{11} cm^2eV^{-1}. Like the dry oxide and N_2O grown the D_{it} increases but at about 0.15 eV the D_{it} of the NO annealed sample crosses the D_{it} of the N_2O grown and is higher and continues to be higher as we probe closer to the conduction band edge and at 50 meV it shows D_{it} of about 1.4×10^{13} cm^2eV^{-1} which is the second highest D_{it} of all the samples at 50 meV. This demonstrates the limited information obtained if CV analysis is only performed at room temperatures. The SEO shows similar D_{it} at 0.4 eV as the NO annealed sample of about 1.5×10^{11} cm^2eV^{-1}. Because of the high series resistance at

50 K we consider the 75 K data instead. The SEO sample shows the lowest D_{it} at 0.1 eV of all the samples of about 5.2×10^{11} cm^2eV^{-1} which is the lowest increase in D_{it} towards the conduction band edge of all the samples. The AlN sample shows the lowest D_{it} of all the samples at 0.4 eV of about 8.2×10^{10} cm^2eV^{-1} but as we probe closer to the conductance band edge the D_{it} increases rapidly and at 50 meV it shows D_{it} of about 9.1×10^{12} cm^2eV^{-1} right below the trap density in the N_2O grown oxide. The Al_2O_3 sample shows similar D_{it} to the N_2O sample at 0.4 eV of about 3.8×10^{11} cm^2eV^{-1} and at 50 meV the D_{it} is about 3.5×10^{12} cm^2eV^{-1} which is the lowest of all samples at 50 K. However, if the trend of the SEO sample would continue we expect it to have the lowest D_{it} at 50 K.

As mentioned above the NI traps contribute to the frequency dispersion in CV and thereby to the D_{it} at low temperatures (50 K, 75 K and 125 K) while the OX traps are responsible for most of the the frequency dispersion at 200 K and 300 K. The OX traps also contribute to the D_{it} at lower temperatures but mainly in the dry oxide sample. The D_{it} graph agrees very well with the observations made by conductance analysis. There the NI trap density is highest in the NO grown sample as shown in figure 5.2. In the D_{it} plot in figure 5.9 the NI trap contributes to the D_{it} curve at low temperatures corresponding to energies close to the conduction band edge. We observe that the NO sample has the highest D_{it} of all samples at 50 meV which agrees very well with the conductance data.

It is evident that CV measurements at room temperature do not detect the NI traps which results in a severe underestimation of the D_{it} when approaching the conduction band edge. It is very well established that high density of interface traps is responsible for low mobility in SiC MOSFETs. When CV analysis is made at room temperature the density of OX traps is estimated and this density is already very low in NO treated oxides. The D_{it} in the SEO sample is very similar to the D_{it} in the NO grown oxide when analyzed at room temperature. However, the field-effect mobility in SEO based MOSFETs is about three to four times higher than in MOSFETs based in nitrided oxides. This difference cannot be explained by a difference in D_{it} (or density of OX traps) at room temperature. If the difference is due to density of interface traps then the NI trap is the main contributor. One cannot exclude that other mechanism can explain the difference in mobility but the NI trap is a probable cause.

Finally it should be mentioned that the D_{it} plot in figure 5.9 is useful when comparing trap density in differently prepared oxides. However, one should not take the exact numbers regarding D_{it} and the energy range too seriously. The D_{it} extraction assumes the traps are interface traps

that communicate with the SiC conduction band through thermal emission according to equation 4.1. The electron capture cross section is assumed to be constant and the value 1.5×10^{-15} cm^2 is used in this analysis. In the case of the NI trap it is clear that this analysis gives a very wide energy range which does not match the surface potential when the NI signal is observed. Furthermore the electron capture cross sections extracted from such analysis are in some cases way too large to be physically reasonable. From analysis in papers I and II it is evident that the NI trap is interacting with the SiC conduction band to a some extent by tunneling and can be regarded as a near-interface trap [14], [77]. A portion of the OX traps are also near-interface traps of which the electron emission does not follow equation 4.1. So, it is evident that the D_{it} plot in figure 5.9 should be discussed with caution but the analysis is still valid for a comparison of the relative densities of interface traps in differently prepared oxides.

5.3 Thermal Dielectric Relaxation Current

The AlN and Al_2O_3 samples are very sensitive to charge injection and leakage and are therefore excluded from TDRC analysis as they would either leak significantly during the charging phase and due to high charge injection would shift the flatband voltage causing the effective electric field applied during the charging phase to be reduced. It should be noted that the TDRC signal is an additional estimation of the OX traps since the NI traps are too fast and escape detection in TDRC analysis [76].

Figure 5.10 shows the TDRC signal measured at differently applied charging voltages of all the SiO_2 samples. The dry oxide (fig.5.10.a) shows the largest signal. Both O1 and O2 humps are clearly visible. The N_2O grown sample (fig.5.10.b) shows about 3x lower TDRC signal that of the dry oxide. The O1 and O2 have both been suppressed and form a more broad TDRC signal. The NO annealed (fig.5.10.c) shows even lower TDRC signal then the N_2O sample or about 2x lower and about 6x lower than the dry oxide. The O1 and O2 peaks are both clearly visible. While both O1 and O2 peaks have been suppressed significantly the O2 has been suppressed more than the O1 peak suggesting that NO annealing effects the deeper O2 traps more than the O1 traps. The SEO sample (fig.5.10.d) shows by far the lowest TDRC signal and is below 0.05 nA/cm^2, that is about 3x lower than the NO annealed sample. The signal is so low that no structure of O1 or O2 are visible. The small rise in the TDRC signal at about 225 K is due to small leakage that occurred while the TDRC measurements were performed on the SEO sample, however, the leakage is small enough to not effect the

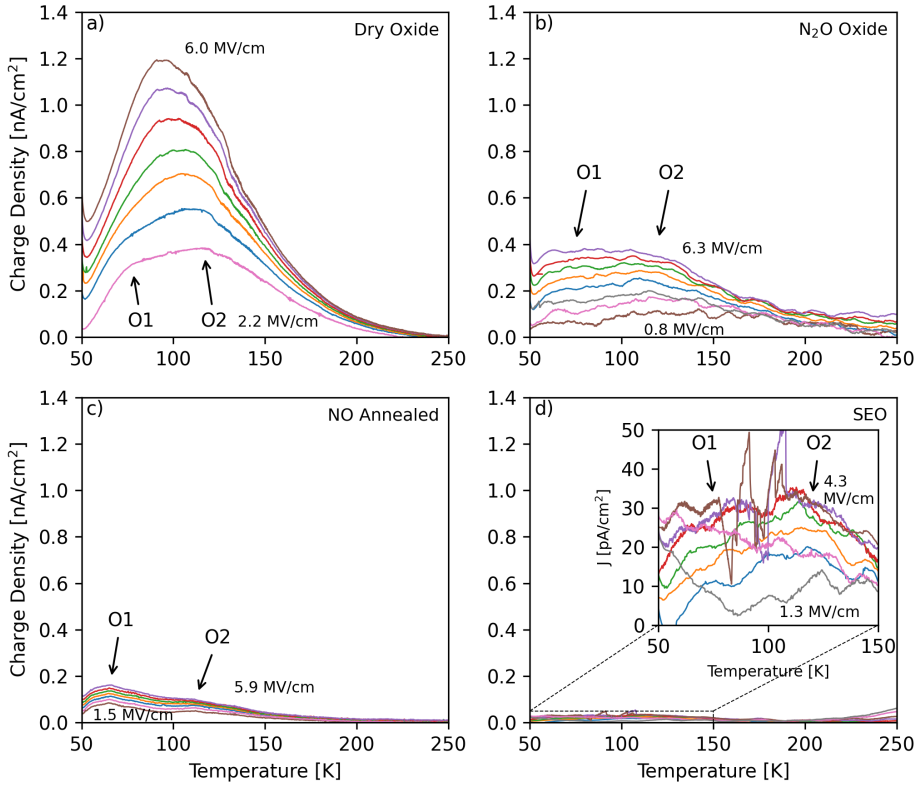

Figure 5.10: TDRC spectra from 50 to 250 K of a) dry oxide, b) N_2O oxide, c) NO annealed oxide and d) sodium enhanced oxide with differently applied charging voltages while cooling. d) Shows zoomed subplot of the TDRC signal in the SEO sample because the signal is so small. The bias corresponds to the accumulation region and the field across the oxide during charging in different oxides is of similar magnitude

overall analysis of the TDRC signal.

Figure 5.11 shows the extracted number density of traps thermally emitted per area as function of the electric field across the oxide during charging while the samples were cooled to cryogenic temperatures. The dry oxide shows the highest number of electrons emitted with about 5.7×10^{12} cm^{-2} at 4 MV/cm applied charging field. The N_2O grown sample shows lower electron emission throughout the spectra or about 2.6×10^{12} cm^{-2} at 4 MV/cm electric field. The NO annealed is even lower than the N_2O grown sample with about 7.6×10^{11} cm^{-2} at 4 MV/cm and SEO has the lowest density of emitted electrons of 3.1×10^{11} cm^{-2} at 4 MV/cm.

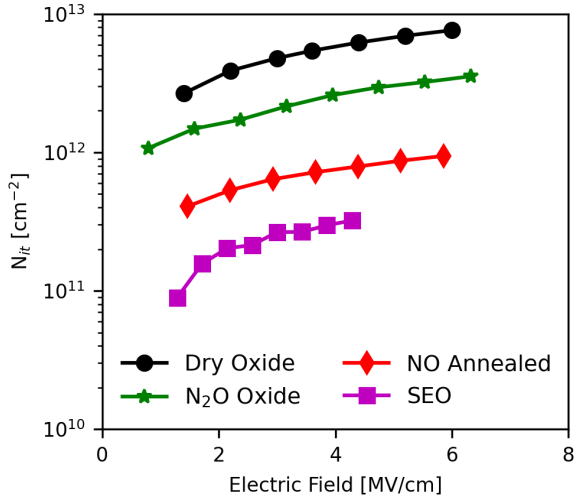

Figure 5.11: Number density of trapped electrons in interface states as a function of the electric field across the oxide during charging of all SiO_2 samples extracted from the TDRC spectra in figure 5.10.

5.4 Subthreshold Slope and Mobility

Figure 5.12 shows the drain source current as a function of gate voltage and the field-effect mobility as a function of gate voltage of MOSFETs using a dry oxide, N_2O grown and SEO gate oxides. We did not have access to NO, AlN or Al_2O_3 MOSFETs for comparison in this study. The reported peak mobility of NO annealed oxides is in the range of 35-50 cm^2/Vs for low doped p-type epilayers. The subthreshold slope is extracted from figure 5.12 a). The slope extracted for the dry oxide gives 2365 mV/dec with peak field-effect mobility (μ_{FE}) of 5 cm^2/Vs, the N_2O oxide gives a slope of 417 mV/dec with peak μ_{FE} of 34 cm^2/Vs and SEO given a slope of 281 mV/dec and peak μ_{FE} of 71 cm^2/Vs. The subthreshold slope (S) is an indication of the interface states density which increases with higher S value. In this case there is a correlation between high S value and low mobility which is expected if interface traps limit the field-effect mobility.

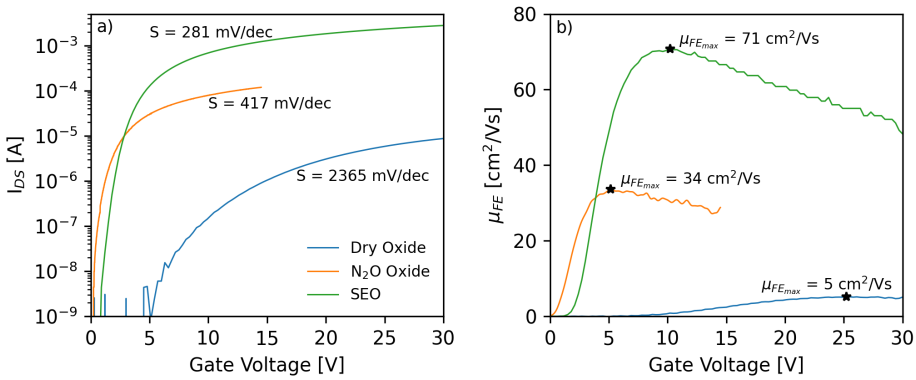

Figure 5.12: Drain source current and field-effect mobility as function of applied gate voltage of dry-, N_2O grown and sodium enhanced oxides. Drain source voltage is 0.1 V. The subthreshold slope for each sample is indicated in figure a) and peak mobility is indicated in figure b).

5.5 Scanning Transmission Electron Microscopy and Electron Energy Loss Spectroscopy

Figures 5.13 and 5.14 show the STEM and EELS intensity of the SiC/Al_2O_3 and SiC/AlN interfaces respectively. The EELS plots show spectroscopically intensity of the Si, N, O, Al, and C signals presented as linescans. The transitions from the SiC to the dielectric are clearly observed, with Al and O replacing Si and C (figure 5.13 b)), and Al and N replacing the same (figure 5.14 b)). For the Al_2O_3 sample, the O is seen to be introduced in the dielectric, and not detected in the SiC. For the AlN sample, the O signal is extremely low, barely detectable, and only in the AlN, not in the SiC. The presence of SiO_2 was neither observed from the STEM images or the EELS linescans. Linescans across the interface for both samples revealed relatively sharp interfaces and with an O-presence only in the dielectric, where Si was not observed. Additionally, the fine-structure comparison indicates that the structures do not suffer from inclusions of native oxidation or islands at the interface. This can be compared to the study by Serin et al. [78], where O inclusion in AlN would affect the fine-structure of N, which is not observed.

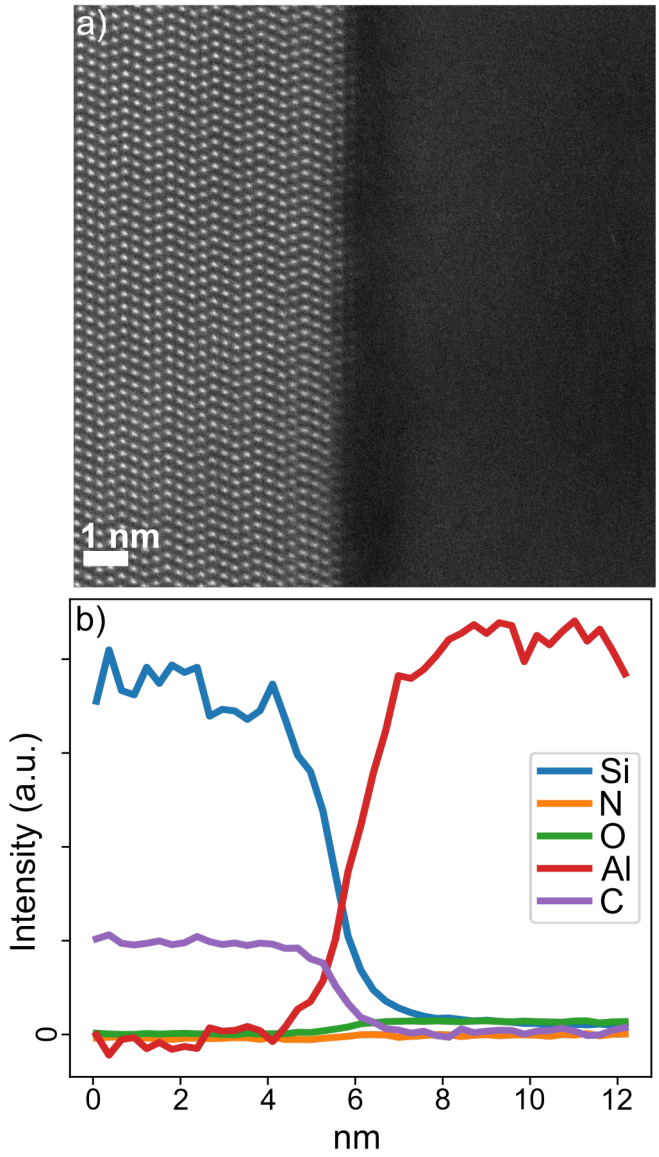

Figure 5.13: a) STEM image of the SiC/Al_2O_3 interface where the Al_2O_3 was grown using the hot plate method. The image shows the 4H-SiC periodic atomic structure and the amorphous Al_2O_3 that appears dark. b) EELS intensity data of the SiC/Al_2O_3 interface. Credit to Dr. Axel R. Persson, Linköping University, see paper 7.

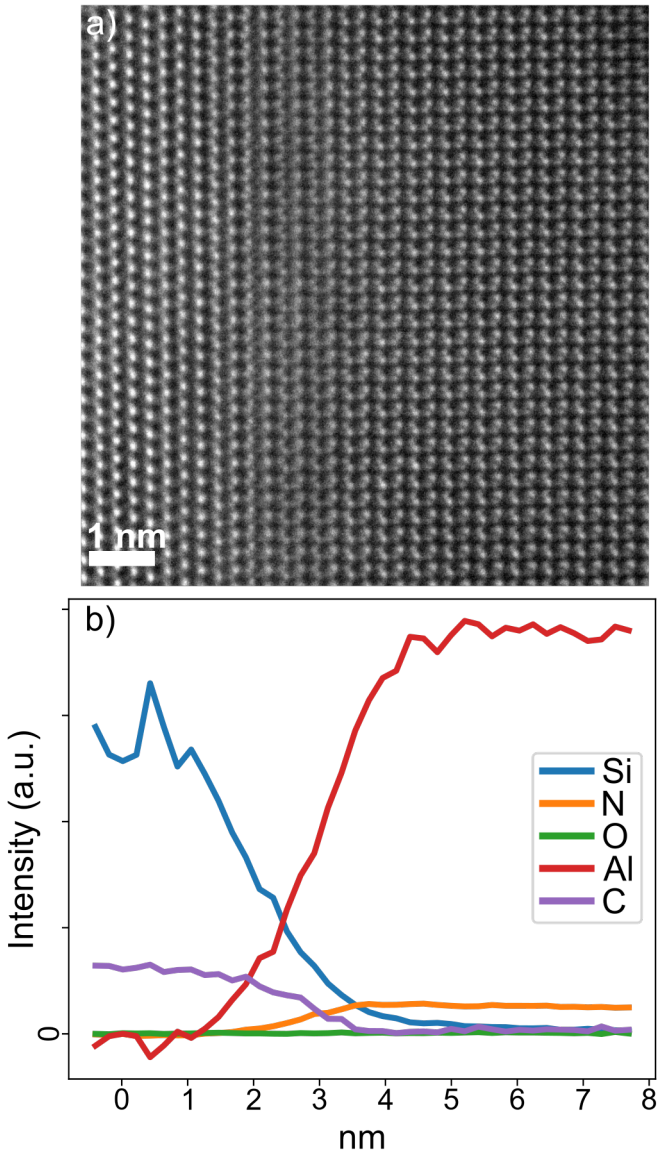

Figure 5.14: a) STEM image of the SiC/AlN interface grown using MOCVD. The images shows the 4H-SiC atomic structure transitioning into the 2H-AlN. b) EELS intensity data of the SiC/AlN interface. Credit to Dr. Axel R. Persson, Linköping University, see paper 7.

Chapter 6

Conclusion and Discussion

In this study we have investigated the SiC/dielectric interface using a variety of different electrical analysis methods on few different dielectrics.

The SiC/SiO_2 dielectric interface shows a strong reduction of the trap density when NO annealing is introduced into the oxide growth processing. However, a trap, noted as NI, is promoted as a result of the NO annealing. This trap is also visible in dry SiO_2 and N_2O grown samples, but with weaker signal intensity. At first glance the NI trap appears to be related to the nitridation of the SiC/SiO_2 interface since the NI signal increases in strength with more nitridation. However, electrical analysis of SiC/high-κ dielectrics interfaces such as SiC/AlN and SiC/Al_2O_3 MIS capacitors tell a different story.

The SiC/AlN interface is of particular interest as the lattice parameters of AlN and SiC are only 1.2% mismatched. This will ideally form smooth transition from SiC to AlN in the MIS structure, and is beforehand expected to result in an interface with very low density of interface traps. Electrical analysis of the SiC/AlN interface does show significant reduction in the density of interface traps. However, the NI trap is also present at the SiC/AlN interface.

The SiC/Al_2O_3 sample also showed significant improvements in the density of interface traps as the AlN. Again, the NI trap is also present at the this interface.

The fact that the NI trap is present at the interface of SiC and three different dielectrics with different energy band offsets suggests that the NI trap is not related to the dielectric used but is native to the SiC surface.

Introducing sodium in the growth process of the SiO_2 oxide enhances the growth rate of the oxide and simultaneously reduces the density of interface traps through-out the D_{it} vs. trap energy spectra. Furthermore, the NI trap is not detected at the interface. This suggests that sodium passivates not only the slow traps in the SiC bandgap but also the NI trap.

The physical origin of the NI trap is still unknown but for the sake of speculation it might be related to the SiC wafer 4° off cut as it is one of

few common factors between the wafer pieces used to fabricate the MOS capacitors. H_2 etching of the SiC Si-face with 4° off cut has shown to smoothen the surface and recent studies report enhanced inversion channel mobility in MOSFETs made using the H_2 etching prior to the dielectric deposition [6].

6.1 Future Outlook

Even if the SEO oxide shows the best results of all the samples tested in this work it is not the solution to the poor inversion channel mobility in SiC MISFETs due to previously discussed problems with mobile ions within the oxide. However, the mechanism of passivation of the NI trap in such oxides is still unknown and has to be further studied. The AlN and Al_2O_3 show promising interface quality and need to be studied more as high-κ dielectric stacked with SiO_2 are of special interest and can provide high interface quality.

Fabrication of samples using the same oxide growth methods but with different wafer off axis cut (4° to on-axis) might show difference in the NI signal strength in the conductance spectroscopy if the NI trap is related to the off cut.

Chapter 7

Summary of The Appended Papers

We have studied traps at the SiC/dielectric interface using various dielectrics on 4H-SiC using different electrical analysis methods. Following is a summary of all published and pending papers and my contributions to each paper.

Paper I **Near-Interface Trap Model for the Low Temperature Conductance Signal in SiC MOS Capacitors With Nitrided Gate Oxides**

Fast traps were detected in nitrided oxide using conductance spectroscopy at cryogenic temperatures. A model is developed to model the conductance signal and extract physical parameters of the fast traps.

My contribution: Did all the measurements and wrote the experimental details chapter and part of the experimental results.

Paper II **A method for characterizing near-interface traps in SiC metal–oxide–semiconductor capacitors from conductance–temperature spectroscopy measurements**

Fast traps detected in NO annealed and NO grown oxides. Model from paper I is expanded upon and the physical location of the traps are extracted from the model and were determined to be tunnelling to and from traps very close to the SiC conduction band edge.

My contribution: Did all the measurements and wrote the experimental details chapter.

Paper III **Observation of Fast Near-Interface Traps in 4H-SiC MOS Capacitors Using Capacitance Voltage Analysis at Cryogenic Temperatures**

Fast traps were detected using capacitance voltage measurements at cryogenic temperatures in NO annealed and dry oxides. The importance of density of interface trap analysis from room temperature and cryogenic temperatures is shown and the underestimation from Hi-Lo extraction at room temperature.

My contribution: Did all the measurements, did the data analysis and wrote the paper.

Paper IV **Detection of near-interface traps in NO annealed 4H-SiC metal oxide semiconductor capacitors combining different electrical characterization methods**

Various different electrical characterization methods are applied to dry and NO annealed oxides to detect fast traps at the SiC/SiO_2 interface. Extraction of density of interface traps from capacitance voltage and conductance spectroscopy are compared. Advantages and limitations of each electrical characterization method is discussed.

My contribution: Did all the measurements, did the data analysis and wrote the paper.

Paper V **Passivation of very fast near-interface traps at the 4H-SiC/SiO_2 interface using sodium enhanced oxidation**

Capacitance voltage and conductance spectroscopy analysis is used to detect fast traps in NO and sodium enhanced oxides (SEO). No fast traps were detected in SEO by either method suggesting passivation of fast traps using sodium. Density of interface traps is compared using CV analysis.

My contribution: Did all the measurements, did the data analysis and wrote the paper.

Paper VI **Improvement of Channel Mobility in 4H-SiC MOSFETs correlated with Passivation of Very Fast Interface Traps Using Sodium Enhanced Oxidation**

Capacitance voltage and conductance spectroscopy measurements were made to detect fast NI traps in dry, N_2O, NO and SEO. Subthreshold and mobility measurements are done on MOSFETs fabricated using the SEO method. Results show the absence of the NI trap in the SEO and 3-4 times higher mobility in MOSFETs fabricated using the SEO method.

My contribution: Did all the measurements, did the data analysis and wrote the paper.

Paper VII **Observations of very fast traps at the SiC/high-κ dielectric interface**

Fast traps were detected using capacitance voltage measurements and conductance spectroscopy at cryogenic temperatures in high-κ dielectrics at the SiC/dielectric interface. This suggests that the very fast NI trap is native to the SiC epilayer and not the SiO_2 as previously suggested.

My contribution: Did all the electrical measurements, did the electrical data analysis and wrote most of the paper.

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Abbreviations

AC	Alternating Current
ALD	Atomic Layer Deposition
AlN	Aluminium Nitride
Al_2O_3	Aluminium Oxide
CVD	Chemical Vapor Deposition
CV	Capacitance Voltage
DC	Direct Current
EELS	Electron Energy Loss Spectroscopy
GaN	Gallium Nitride
MBE	Molecular Beam Epitaxy
MIS	Metal Insulator Semiconductor
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOCVD	Metal-Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N	Nitrogen
N_2O	Nitrous Oxide
NI	Very Fast Interface Traps
NO	Nitric Oxide
OX	Slow Interface Traps
PECVD	Plasma Enhanced Chemical Vapor Deposition
SEO	Sodium Enhanced Oxidation
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
STEM	Scanning Transmission Electron Microscopy
TDRC	Thermal Dielectric Relaxation Current

Symbol Index

A	Area [m^2]
C_{fb}	Flatband Capacitance [F]
C_{hi}	Capacitance of Higher Frequency [F]
C_i	Accumulative Capacitance of the Insulator [F]
C_{lo}	Capacitance of Lower Frequency [F]
C_m	Measured Capacitance [F]
C_p	Parallel Capacitance [F]
C_s	Semiconductor Capacitance [F]
C_{theory}	Theoretical Capacitance [F]
D_{it}	Density of Interface Traps [$eV^{-1}m^{-2}$]
E	Electric Field [V/m]
E_C	Energy of Conduction Band [eV]
E_F	Fermi Energy [eV]
E_i	Intrinsic Energy [eV]
E_T	Energy of a Trap [eV]
E_V	Energy of Valance Band [eV]
f	Frequency [Hz]
G_m	Measured Conductance [S]
G_p	Parallel Conductance [S]
j	Complex Number $\sqrt{-1}$
k_B	Boltzmann Constant [JK^{-1}]
L_D	Debye Length [m]
N_C	Effective Density of States in the Conduction Band [m^{-3}]
N_D	n-type Donor Concentration [m^{-3}]

N_{it}	Number of Traps at the SiC/Insulator Interface [m^{-3}]
q_e	Elementary Charge of Electron [C]
t_i	Insulator thickness [m]
T	Temperature [K]
V	Voltage [V]
v_s	Band Bending [eV]
v_{th}	Thermal Velocity [m/s]
$\mathcal{A}$	Area Under TDRC Signal Curve [A·K/m^2]
$\alpha(\sigma_s)$	Standard Deviation Factor
β	Ramp Rate [K/s]
ϵ_0	Permittivity of Vacuum [F/m]
ϵ_i	Permittivity of The Insulator [F/m]
ϵ_{SiC}	Permittivity of SiC [F/m]
η	$v_s - \langle v_s \rangle$ [eV]
κ	Dielectric Constant of the Insulator
μ_{FE}	Field-Effect Mobility [cm^2/Vs]
σ_c	Capture Cross Section [m^2]
σ_s	Standard Deviation [eV]
τ	Time Constant [s]
ψ_s	Surface Potential [eV]
ω	Angular Frequency [rad/s]

Chapter 8

Appended papers